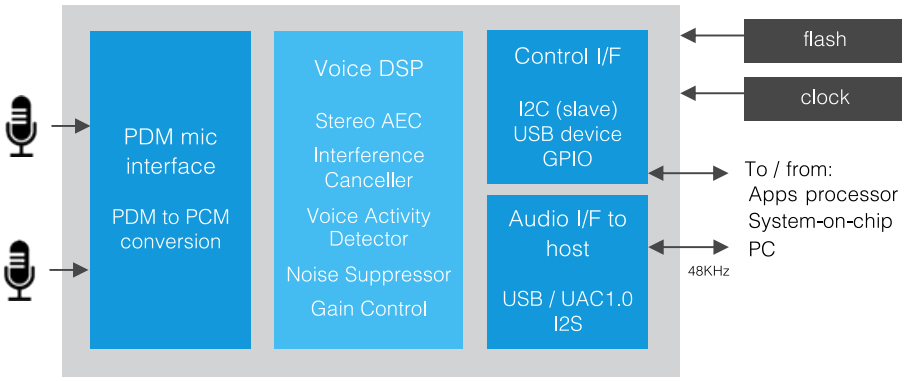
XVF3510-QF60 FAR-FIELD VOICE PROCESSOR

VOCALFUSION™

DATASHEET

FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS

- Smart TVs
- Set-top boxes
- TV accessories

TWO-MICROPHONE FAR-FIELD VOICE PROCESSOR

- 2 MEMS microphone array with 71mm spacing
- Acoustic Echo Cancellation of the audio output supporting 150ms echo tail length
- Interference canceller for the suppression of point noise sources
- Audio interfaces
  - High speed USB2.0 compliant device supporting USB Audio Class 1.0 at 48kHz sample rate
  - I2S audio interface, 48kHz sample rate
- System control options
  - I2C serial control interface
  - USB control interface
- Reference audio signal via USB or I2S
- Switchable stationary noise suppressor
- Adjustable gain over a 60dB range
- Output range limiter
- Fast QSPI boot from flash, or SPI boot from host processor
- JTAG boundary scan for production testing
- 7mm x 7mm 60pin QFN package

CONTENTS

1. XVF3510 AUDIO PROCESSING PIPELINE

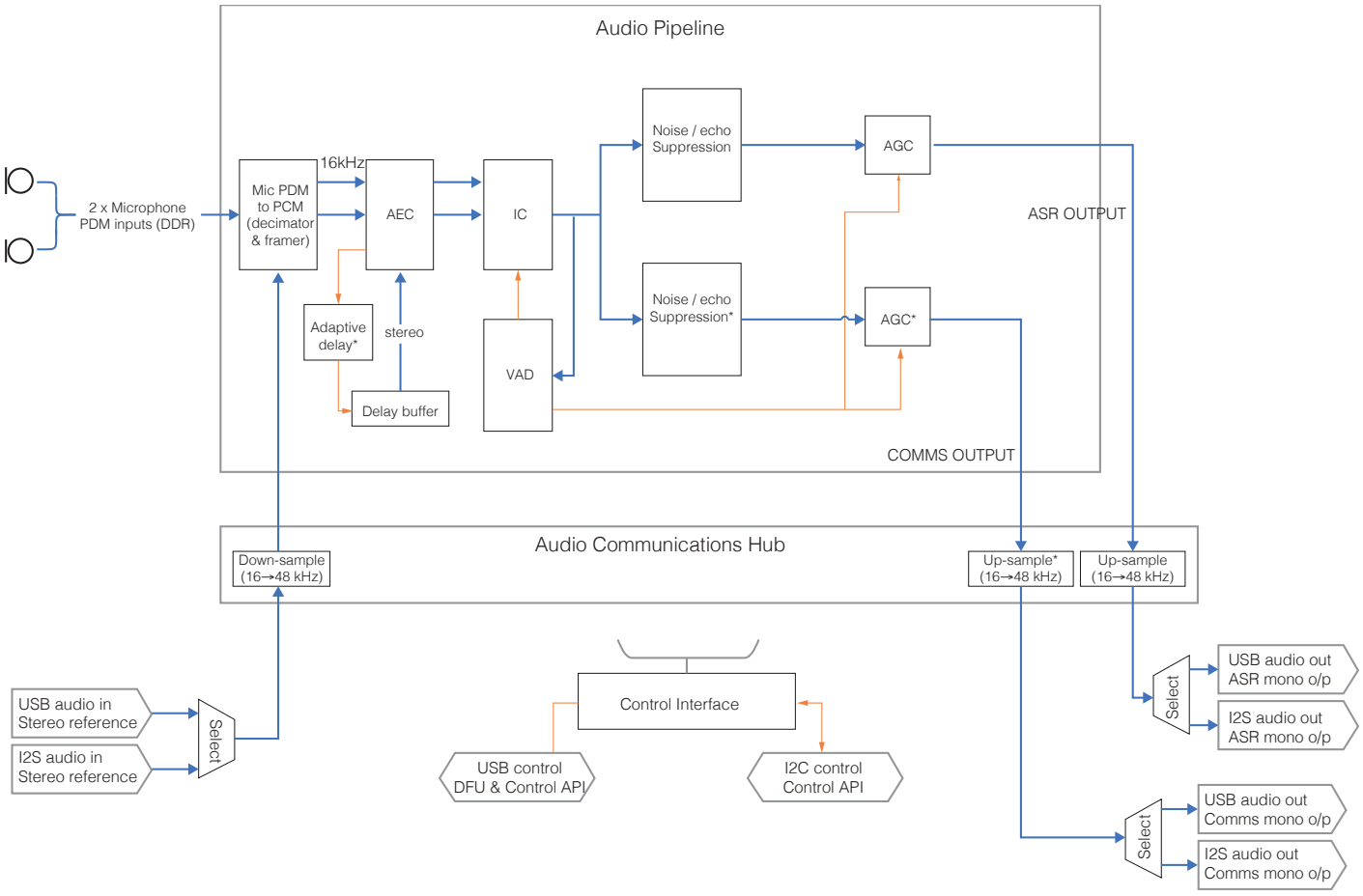


Figure 1: XVF3510 block diagram

The XVF3510 audio processing pipeline takes inputs from a pair of MEMS PDM output microphones and processes them to create an audio stream suitable for use in Automatic Speech Recognition based applications. Signal to noise ratios are enhanced by a set of complimentary signal enhancement and noise reduction processes:

Acoustic Echo Cancellation: enables the XVF3510 to detect voice signals in the presence of high volume stereo audio from the product in which it is integrated. Microphone audio inputs are converted to PCM and then passed directly to an Acoustic Echo Cancellation unit. This unit takes a stereo reference signal that is the audio being output by the product and evaluates the four echo characteristics of the room separately from the left and right speakers to the left and right microphones. The echo canceller continuously removes the echo from the microphone audio input and adapts to changes in the room characteristics created by normal events such as people moving about in the room.

- Interference Cancellation: point noise sources such as cooker hoods, washing machines, or entertainment devices such as radios for which there is no reference audio signal available are suppressed by a directional Interference Canceller.
- Noise Suppression: stationary noise sources (i.e. noise sources with frequency characteristics that do not change rapidly over time) are suppressed in all directions. The attenuation applied is adjustable.

2. PIN DIAGRAM

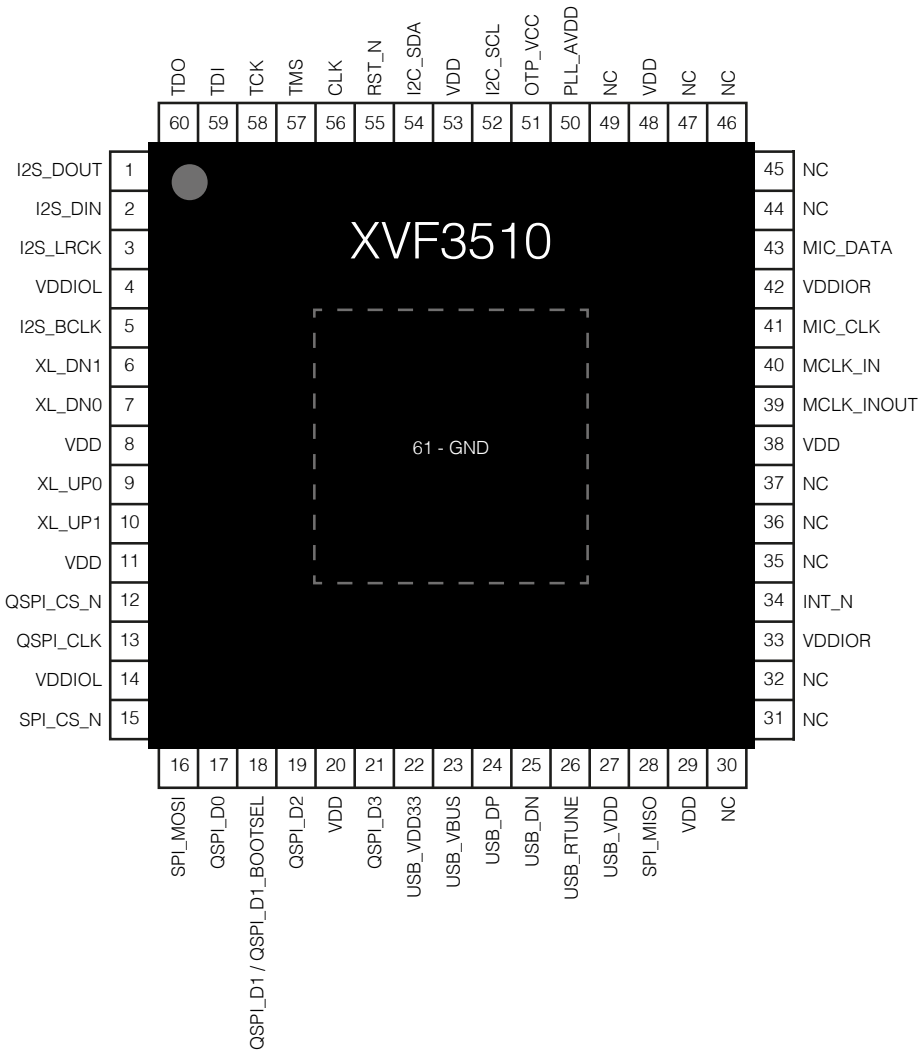


Figure 2: Pin diagram

Figure 2 shows the pinout of the XVF3510 including all optional interfaces.

Pins marked NC are internally connected and should remain unconnected.

2.1. SIGNAL DESCRIPTION

This section lists the signals available on the XVF3510-QF60 device.

Table 1: Boot and JTAG pins

Name	Description	Pin
QSPI_CS_N	QSPI Chip Select. This pin should be pulled high externally to the device using a 4.7k ohm resistor.	12
QSPI_D0	QSPI Data Line 0	17
QSPI_D1 or QSPI_D1_BOOTSEL	QSPI Data Line 1 and boot selection. If this pin is tied high via a 4.7k ohm resistor on startup, the device will start in SPI slave boot mode. If the pin is left floating, pulled low or connected to a quad SPI D1 pin, the device will start in QSPI master mode and attempt to boot from a local QSPI flash memory.	18
QSPI_D2	QSPI Data Line 2	19
QSPI_D3	QSPI Data Line 3	21
QSPI_CLK	QSPI Clock	13
SPI_CS_N	SPI Chip Select. This pin should be pulled high externally to the device using a 4.7k ohm resistor.	15
SPI_MOSI	SPI Master Out Slave In	16
SPI_MISO	SPI Master In Slave Out	28
MIC_DATA	Mic array data. Two standard PDM MEMS microphones should be connected to this pin by setting one as the left microphone and one as the right.	43
MIC_CLK	Mic array clock. This 3.072MHz clock output drives the data capture from the PDM microphones.	41
TDO	JTAG Test data output. This pin has a weak pull down resistor applied during and after reset until the device has booted. Boundary scan capability is provided in the device - contact XMOS for details.	60
TDI	JTAG Test data input. This pin has a weak pull up resistor applied during and after reset until the device has booted. Boundary scan capability is provided in the device - contact XMOS for details.	59
TMS	JTAG Test mode select. This pin has a weak pull up resistor applied during and after reset until the device has booted. Boundary scan capability is provided in the device - contact XMOS for details.	57
TCK	JTAG Test clock. This pin has a Schmitt tigger input and a weak pull down resistor applied during and after reset until the device has booted. Boundary scan capability is provided in the device - contact XMOS for details.	58
RST_N	Device reset - active low. This pin has a Schmitt trigger input and an internal weak pull up resistor.	55
CLK	PLL reference clock. This input pin has a Schmitt trigger input. A 24MHz reference clock must be provided to this pin.	56

Name	Description	Pin
MCLK_IN MCLK_INOUT	I2S master clock. When I2S connectivity is used, a 24.576MHz clock signal synchronised with the I2S_BLCK must be provided to allow microphone data processing to be fully matched to the host processor data rate. These pins must be connected to MCLK_INOUT outside the device.	39 40

Table 2: Power pins - pins that must all be connected regardless of the boot image used

Name	Description	Pin
PLL_AVDD	PLL analog power. This 1.0V (nominal) supply should be separated from the other supplies at the same voltage by a low pass filter.	50
USB_VDD	USB digital core power. This 1.0V (nominal) supply may be powered directly by the same regulator use to provide VDD. This pin must be connected even if the USB interface is not used.	27
VDD	Digital core power. 1.0V (nominal)	8 11 20 29 38 48 53
VDDIOL	Digital I/O power (left)	4 14
VDDIOR	Digital I/O power (right)	33 42
OTP_VCC	OTP power	51
USB_VDD33	USB tile analog power	22
GND	Ground	61 (Paddle)

Table 3: XMOS link pins

Name	Description	Pin
XL_DN1	XMOS link, downlink bit 1. See Section 6.2 for connection details.	6
XL_DN0	XMOS link, downlink bit 0. See Section 6.2 for connection details.	7
XL_UP0	XMOS link, uplink bit 0. See Section 6.2 for connection details.	9
XL_UP1	XMOS link, uplink bit 1. See Section 6.2 for connection details.	10
INT_N	Active low interrupt output. This pin is reserved for future use as an applications processor interrupt signal.	34
NC	Pin reserved for future use. Do not connect or short together.	30 31 32 35 36 37 44 45 46 47 49

Table 4: USB pins - pins that must be connected for products that use the USB interface

Name	Description	Pin
USB_DP	USB positive data line	24
USB_DN	USB negative data line	25
USB_RTUNE	USB tuning resistor. Connect a 43.2 ohm resistor to ground	26
USB_VBUS	USB VBUS Voltage - not used by XVF3510, leave unconnected. Contact XMOS for further information on self-powered architectures.	23

Table 5: I2S pins - pins that must be connected when using the I2S Slave interface

Name	Description	Pin
I2S_DOUT	I2S data out. Processed audio output from the microphones is passed to the host processor during the left channel phases of the I2S communication. The right channel output is undefined in this release but reserved for future use. Signals observed on this output should be ignored.	1
I2S_DIN	The host processor passes stereo reference audio signals to the device on this pin.	2
I2S_LRCK	I2S left-right clock.	3
I2S_BCLK	I2S bit clock. All samples over I2S are delivered and received assuming a 32bit frame format. The I2S_BLCK signal should be 1.536MHz and fully synchronised with I2S_LRCK.	5
MCLK_IN	I2S master clock. When I2S connectivity is used, a 24.576MHz clock signal synchronised with the I2S_BLCK must be provided to allow microphone data processing to be fully matched to the host processor data rate. This pin must be connected to MCLK_INOUT outside the device.	39
MCLK_INOUT	I2S master clock. When I2S connectivity is used, a 24.576MHz clock signal synchronised with the I2S_BLCK must be provided to allow microphone data processing to be fully matched to the host processor data rate. This pin must be connected to MCLK_IN outside the device.	40
I2C_SCL	I2C serial clock line	52
I2C_SDA	I2C serial data line	54

3. CONTROL, AUDIO AND MICROPHONE INTERFACE SUPPORT

During operation of a typical product, the XVF3510 is connected either directly to an applications processor within the product or remotely to a device with general purpose compute capability. The connections required are:

- Processed microphone output.
- Stereo reference audio input if the product plays audio through speakers.
- A control interface if the system requires it.

These connections are provided by USB, I2S and I2C interfaces, shown in Table 7.

Table 7: XVF3510 configurations

Configuration	Audio Out	Control	Reference	Notes
USB xk_vf3510_l71_usb	USB	USB	USB	Pins 1, 2, 3, 5, 52, 54 are not used and should not be connected
I2S Slave xk_vf3510_l71_i2s_slave	I2S	I2C	I2S	Pins 24, 25, 26 are not used and should not be connected. USB power pins (22, 27) should still be connected to the appropriate power supply.
USB / I2S xk_vf3510_l71_hybrid_usb_i2s	I2S	USB	I2S	Pins 1, 52, 54 are not used and should not be connected

Each configuration is provided by a separate firmware image, available to registered users on the XMOS website.

3.1. USB

USB Audio Class 1 is used to deliver stereo reference audio to the XVF3510, processed voice audio to the host processor and as a control interface. See Section 5 for details on integrating the USB PHY.

3.2. I2S

A 48kHz I2S interface can be used as an audio transport mechanism, with USB or I2C control.

The XVF3510 acts as an I2S slave receiving reference audio signals from a host via I2S input and providing processed audio output to the host via an I2S output. This bidirectional flow of audio samples must be synchronised to a single set of I2S clocks, see Section 4.1:

Signal	Description	Comment
MCLK_IN	Master clock	24.576MHz clock signal
I2S_BCLK	I2S bit synchronisation clock	3.072MHz clock derived as MCLK/8
I2S_LRCK	I2S sample synchronisation clock	48kHz clock derived as BLCK/64.

The I2S audio samples are transmitted serially with a 1 I2S_BLCK delay between the change of I2S_LRCK phase and the start (MSB) of the audio sample for that channel. This the standard alignment for I2S systems.

3.3. I2C

I2C is used as a control interface. The device I2C address is set to 0x2C. See Section for details on using the Control Interface.

Known Issue: I2C commands will not always be processed if the device is booted as an I2S slave but there are no I2S clocks running. To ensure an I2S clock is running simply record or play from the device (e.g. using Audacity on the connected host processor / computer).

3.4. MICROPHONE INPUT

The XVF3510 is connected to a pair of PDM microphones via a single shared data line and a microphone clock signal. The data input makes use of the left and right channel output capability of standard MEMS microphones. In most microphone products the Left/Right selection pin is tied high for one microphone and low for the other microphone. The XVF3510 reads one microphone on the positive going edge of the microphone clock and the other microphone on the negative going edge of the microphone clock.

The XVF3510 outputs a microphone clock at 3.072MHz, which is fed directly to both microphones. This signal must be used to clock the microphone PDM output to avoid undefined artifacts in the processed audio stream.

Microphones should be placed in the system with a 71mm separation and connected to the product casing in such a way that the audio path to each microphone from outside the product is independent. Contact XMOS for details of other microphone separations.

4. POWER-UP AND RESET

4.1. CLOCKS

The XVF3510 must be provided with a 24MHz system clock on the CLK pin.

Signal	Description	Comment
MCLK_IN	Master clock	24.576MHz clock signal
I2S_BCLK	I2S bit synchronisation clock	3.072MHz clock derived as MCLK/8
I2S_LRCK	I2S sample synchronisation clock	48kHz clock derived as BLCK/64.

4.2. BOOT MODES

On startup and after any reset, the XVF3510 must be booted either using an externally connected QSPI flash memory or by driving a boot image into the device via SPI by a local host processor.

The boot mode is specified using QSPI_D1_BOOTSEL (pin 18). If this pin is tied high via a 4.7k ohm resistor on startup, the XVF3510 will start in SPI Slave boot mode; if the pin is left floating, pulled low or connected to a quad SPI D1 pin, the device will start in QSPI master mode and attempt to boot from a local QSPI flash.

Boot mode	Description	Active pins
QSPI Master	QSPI_D1_BOOTSEL connected to QSPI D1 pin on flash device or QSPI_D1_BOOTSEL pulled low or floating	QSPI_CS_N (12) QSPI_D0 (17) QSPI_D1 (18) QSPI_D2 (19) QSPI_D3 (21) QSPI_CLK (13)
SPI Slave	QSPI_D1 tied high via a 4.7k ohm resistor	SPI_CS_N (15) SPI_MOSI (16) SPI_MISO (28)

4.2.1. QSPI MASTER

If set to boot from QSPI master, the XVF3510 enables the six QSPI pins (see Table 1) and drives the SPI clock at 50MHz. A READ command is issued with a 24-bit address 0x000000.

The XVF3510 expects each byte to be transferred with the least-significant nibble first. Programmers that write bytes into an QSPI interface using the most significant nibble first may have to reverse the nibbles in each byte of the image stored in the QSPI device.

4.2.2. SPI SLAVE

The XVF3510 can be booted from a host applications processor rather than an external flash device, using the slave SPI interface. If set to boot from SPI slave, the XVF3510 enables the three SPI pins (see Table 1) and expects a boot image to be clocked in with the least significant bit first in each transferred byte. Contact your XMOS sales representative for further details on how to incorporate this feature on your product.

4.2.3. QSPI CONFIGURATION FILES

QSPI flash devices require a configuration file (spispec) which describes the device characteristics, such as page size, number of pages and commands for reading, writing and erasing data. This information can be found in the datasheet for the flash device. Many devices available in the market can be described using these configuration parameters; those that cannot are unsupported.

The configuration file for the Adestro AT25SF161 device used in the VocalFusion Dev Kit (XK-VF3510-L71) is shown below. For detailed information on each parameter see the *XMOS Tools User Guide - Add support for a new flash device*.

```
0,                      /* AT25SF161 - Just specify 0 as flash_id */
256,                    /* page size */
8192,                   /* num pages */
3,                      /* address size */
3,                      /* log2 clock divider */
0x9F,                   /* QSPI_RDID */
0,                      /* id dummy bytes */
3,                      /* id size in bytes */
0x1F8601,               /* device id */
0x20,                   /* QSPI_SE */
4096,                   /* Sector erase is always 4KB */
0x06,                   /* QSPI_WREN */
0x04,                   /* QSPI_WRDI */
PROT_TYPE_SR,           /* Protection via SR */
{{0x18,0x00},{0,0}},    /* QSPI_SP, QSPI_SU */
0x02,                   /* QSPI_PP */
0xEB,                   /* QSPI_READ_FAST */
1,                      /* 1 read dummy byte */
SECTOR_LAYOUT_REGULAR,  /* mad sectors */
{4096,{0,{0}}},         /* regular sector sizes */
0x05,                   /* QSPI_RDSR */
0x01,                   /* QSPI_WRSR */
0x01,                   /* QSPI_WIP_BIT_MASK */
```

Figure 3: Adestro AT25SF161 spispec file

4.3. POWER CONNECTIONS

The XVF3510 has the following power supply pins:

- VDD pins for the core logic, including a USB_VDD pin that powers the USB PHY
- VDDIO pins for the I/O lines
- PLL_AVDD pins for the PLL
- A USB_VDD33 pin for the analogue supply to the USB-PHY

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

VDDIO/OTP_VCC and VDD can ramp up independently. In order to reduce stresses on the device, it is preferable to make them ramp up in a short time frame of each other, no more than 50 ms apart. RST_N should be kept low until all power supplies are stable and within tolerances of their final voltage. When RST_N comes up, the processor

will attempt to boot within a very short period of time. If booting from external flash, ensure that there is enough time between before RST_N coming up for the external flash to settle. Power sequencing is summarised in Figure 4.

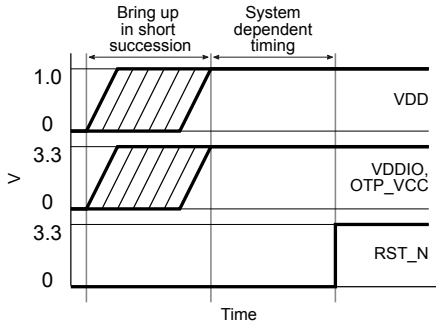


Figure 4: Sequencing of power supplies and RST_N

The PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 ohm resistor and 100nF multi-layer ceramic capacitor) is recommended on this pin.

A single ground pin is provided as the central paddle pin beneath the device in the package. It is a recommended that this is connected by a ring of vias to the board ground plane.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 100nF 0402 for each supply pin). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10uF should be placed on each of these supplies.

4.4. RESET

To reset the XVF3510, pull RST_N low until the power supplies have stabilised to within operating conditions.

4.5. DEVICE FIRMWARE UPGRADE

Device Firmware Upgrade (DFU) is supported for devices that have QSPI flash connected and loaded with a factory firmware image. Sample host code provided as source with the VocalFusion Dev Kit allows DFU to work from the command line or be integrated into a customer's application. If the DFU process fails, the boot process safely falls back to the factory image allowing the user to re-attempt the upgrade. Images loaded via DFU can also be removed allowing the device to revert to the factory image.

DFU is only supported over the USB control interface for the current XVF3510 release. For I2C based designs, booting the XVF3510 over SPI provides a suitable alternative to DFU.

Contact XMOS for further information on DFU support.

5. USB PHY

5.1. USB CONNECTIONS

The integrated USB PHY is used to provide data and control instructions to the XVF3510 device. Table ??? shows the connections required if the device is wholly powered by USB and the device is used to implement a USB-device:

Table 8: USB connections

Name	Description
USB_DP	Connect to USB connector
USB_DN	Connect to USB connector
USB_RTUNE	An external resistor of 43.2 ohm (1% tolerance) should connect USB_RTUNE to ground, as close as possible to the device.
USB_VBUS	Do not connect. A 2.2 uF capacitor to ground is required on the VBUS pin of the connector. A ferrite bead may be used to reduce HF noise.
USB_VDD	1V0 digital supply. This 1V0 (nominal) supply may be powered directly by the same regulator used to power VDD. It is required even if the USB interface is not used.
USB_VDD33	3V3 analogue supply to the USB-PHY.

The XVF3510 firmware only supports bus-powered USB implementations. If you want to add a self-powered USB device into your design, please contact XMOS for further details.

5.2. USB SIGNAL ROUTING AND PLACEMENT

The USB_DP and USB_DN lines are the positive and negative data polarities of a high speed USB signal respectively. Their high-speed differential nature implies that they must be coupled and properly isolated. The board design must ensure that the board traces for USB_DP and USB_DN are tightly matched. In addition, according to the USB 2.0 specification, the USB_DP and USB_DN differential impedance must be 90 Ω.

5.2.1. GENERAL ROUTING AND PLACEMENT GUIDELINES

The following guidelines will help to avoid signal quality and EMI problems on high speed USB designs. They relate to a four-layer (Signal, GND, Power, Signal) PCB.

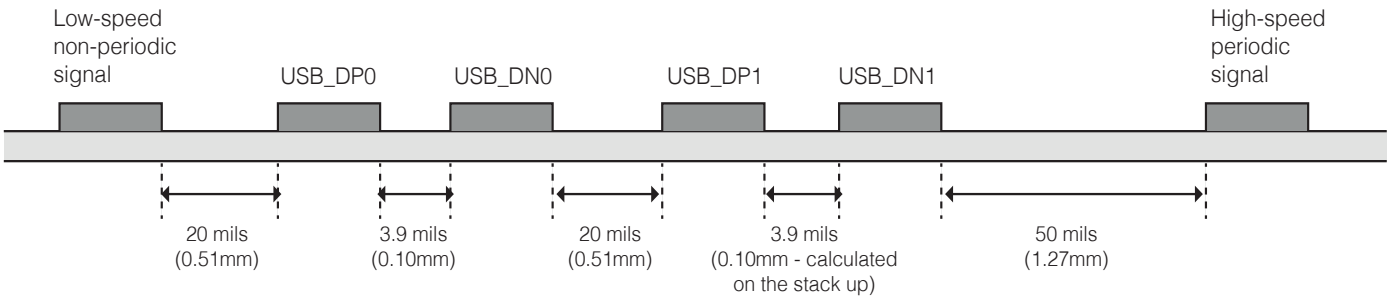


Figure 5: USB trace separation showing low speed signal, two differential pairs and high-speed clock

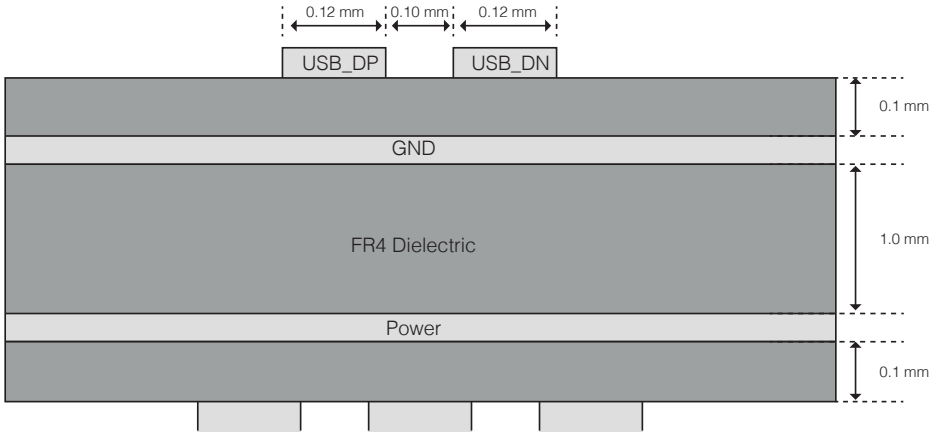


Figure 6: Example USB board stack

For best results, most of the routing should be done on the top layer (assuming the USB connector and XVF3510-QF60 are on the top layer) closest to GND. Reference planes should be below the transmission lines in order to maintain control of the trace impedance.

We recommend that the high-speed clock and high-speed USB differential pairs are routed first before any other routing. When routing high speed USB signals, the following guidelines should be followed:

- High speed differential pairs should be routed together.
- High-speed USB signal pair traces should be trace-length matched. Maximum trace-length mismatch should be no greater than 4mm.
- Ensure that high speed signals (clocks, USB differential pairs) are routed as far away from off-board connectors as possible.
- High-speed clock and periodic signal traces that run parallel should be at least 1.27mm away from USB_DP/USB_DN (see Figure 5).
- Low-speed and non-periodic signal traces that run parallel should be at least 0.5mm away from USB_DP/USB_DN (see Figure 5).
- Route high speed USB signals on the top of the PCB wherever possible.
- Route high speed USB traces over continuous power planes, with no breaks. If a trade-off must be made, changing signal layers is preferable to crossing plane splits.
- Follow the 20 x h rule; keep traces 20 x h (the height above the power plane) away from the edge of the power plane.
- Use a minimum of vias in high speed USB traces.
- Avoid corners in the trace. Where necessary, rather than turning through a 90 degree angle, use two 45 degree turns or an arc.
- DO NOT route USB traces near clock sources, clocked circuits or magnetic devices.
- Avoid stubs on high speed USB signals.

6. JTAG AND XMOS SYSTEM DEBUG

6.1. JTAG MODULE

The JTAG module can be used for boundary scan testing. The JTAG chain structure is illustrated in Figure 7.

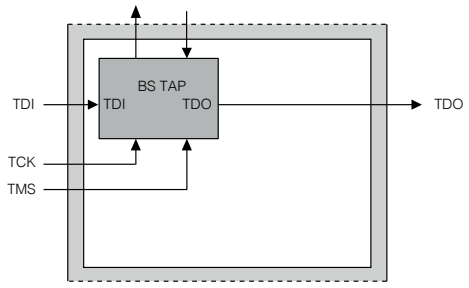


Figure 7: JTAG TAPs

It comprises a single 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. It has a 4-bit IR and 32-bit DR. It also provides access to a chip TAP that is reserved for XMOS internal use. The JTAG module can be reset by holding TMS high for five clock cycles.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified below:

Bit31				Device Identification Register																								Bit0
Version				Part Number																Manufacturer Identity								1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	1	1
0				0				0				0				5				6				3				3			

Figure 8: JTAG IDCODE

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified below:

Bit 31				Usercode Register																								Bit 0
Unused														Silicon Revision														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0				0				0				2				8				0				0				0			

Figure 9: JTAG USERCODE

6.2. XMOS SYSTEM DEBUG

If you intend to design a board that can be used with the XMOS toolchain and XTAG debugger, you will need an XSYS header on your board. Figure Figure 10 shows a decision diagram which explains what type of XSYS connectivity you need. The three subsections below explain the options in detail.

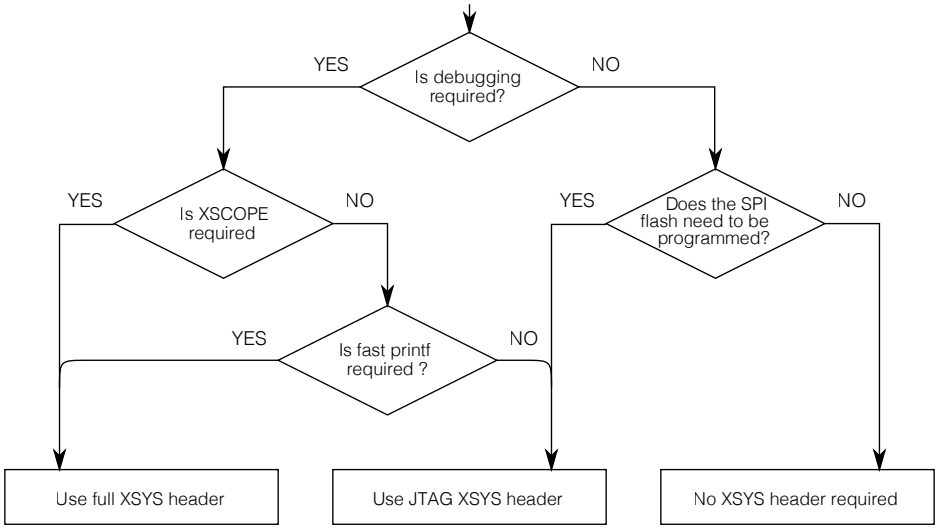


Figure 10: Decision diagram for the XSYS header

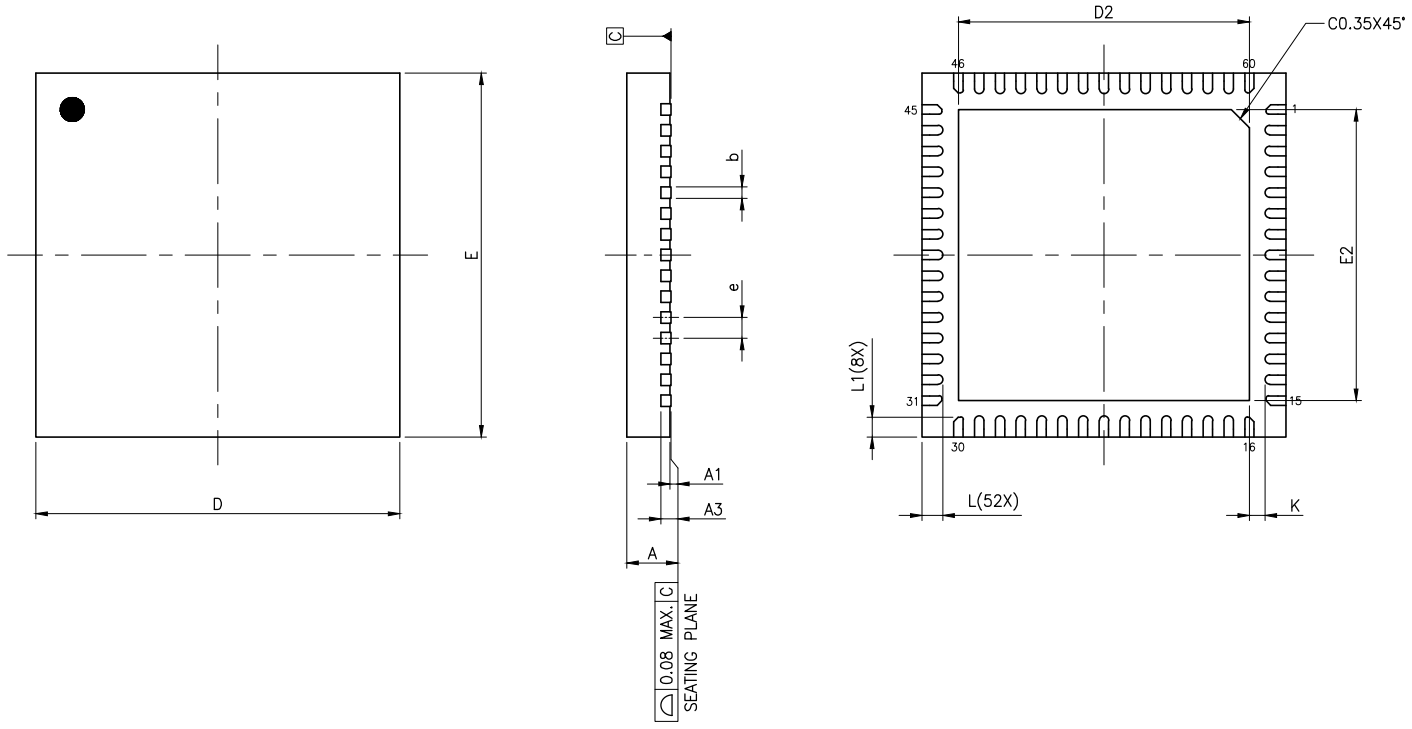
No XSYS header	The use of an XSYS header is optional, and may not be required for volume production designs. However, the XMOS tools expect the XSYS header; if you do not have an XSYS header you must provide your own method for writing to flash and for debugging.
JTAG-only XSYS header	The XSYS header connects to an XTAG debugger, which has a 20-pin 0.1" female IDC header. We advise to use a a male IDC boxed header to guard against incorrect plug-ins. If you use a 90 degree angled header, make sure that pins 2, 4, 6, ..., 20 are along the edge of the PCB. See Table 9 for details of pin connections.
Full XSYS header	For a full XSYS header connect the pins as discussed above, and then connect a 2-wire XMOS Link to the XSYS header. The links can be found in the Signal description table (Section 2.1) labelled XL_UP0, XL_UP1, XL_DN1, XL_DN0.

Table 9: XSYS header pins

Signal	XSYS header pin	No XSYS header	JTAG XSYS header	Full XSYS header
TDI	5		✔	✔
TMS	7		✔	✔
TCK	9		✔	✔
TDO	13		✔	✔
RST_N	15		✔	✔
XL_UP1	6			✔
XL_UP0	10			✔
XL_DN0	14			✔
XL_DN1	18			✔
GND	4 8 12 16 20		✔	✔
NC	1 2 3 11 17 19			

7. PACKAGE INFORMATION

The XVF3510 uses a 60 pin Quad Flat No-leads package (QFN) on a 0.4mm pin-pitch with an exposed ground paddle/ heat slug. The land patterns and solder stencils will depend on the PCB manufacturing process. We recommend you refer to the IPC specification for development of land patterns. This standard aims to achieve desired targets of heel, toe and side fillets for solder-joints.



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	VQFN(Y760)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
D	6.90	7.00	7.10
E	6.90	7.00	7.10
e	0.40 BSC		
K	0.20	—	—

PAD SIZE	228X22* MIL		
JEDEC CODE	N/A		
LEAD FINISH	Pure Tin		PPF
	V		X
SYMBOLS	MIN.	NOM.	MAX.
b	0.15	0.20	0.25
D2	5.50	5.60	5.70
E2	5.50	5.60	5.70
L1	0.33	0.38	0.43
L	0.35	0.40	0.45

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 11: XVF3510-QF60 packaging

7.1. PART MARKING

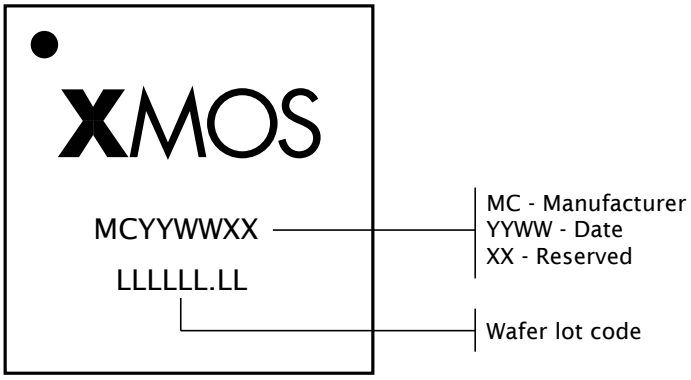


Figure 12: Part marking scheme

7.2. PART ORDERING

Product Code	Marking	Qualification
XVF3510-QF60-C	VSM06C	Commercial

Table 10: Ordering codes

8. ELECTRICAL CHARACTERISTICS

8.1. ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Table 11: Absolute maximum ratings

Symbol	Parameter	MIN	MAX	UNITS	Notes
VDD	Tile DC supply voltage	-0.2	1.1	V	
PLL_VDD	PLL analog supply	-0.2	1.1	V	
VDDIO	I/O supply voltage	-0.3	3.75	V	
OTP_VCC	OTP supply voltage	-0.3	3.75	V	
Tj	Junction temperature		125	°C	
Tstg	Storage temperature	-65	150	°C	
V(Vin)	Voltage applied to any I/O pin	-0.3	3.75	V	
I(XxDxx)	GPIO current	-30	30	mA	
I(VDDIOL)	Current for VDDIOL domain		490	mA	A, B, C
I(VDDIOR)	Current for VDDIOR domain		490	mA	A, B, C
USB_VDD	USB tile DC supply voltage	-0.2	1.1	V	
USB_VDD33	USB tile analog supply voltage	-0.3	3.75	V	
USB_VBUS	USB VBUS voltage	-0.3	5.75	V	
USB_DP	USB DP voltage	-0.3	5.5	V	
USB_DM	USB DM voltag	-0.3	5.5	V	

A: Exceeding these current limits will result in premature aging and reduced lifetime.

B: This current consumption must be evenly distributed over all VDDIO pins.

C: All main power (VDD, VDDIO) and ground (VSS) pins must always be connected to the external power supply, in the permitted range.

8.2. OPERATING CONDITIONS

Table 12: Operating conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIOL	I/O supply voltage	3.135	3.30	3.465	V	
VDDIOR	I/O supply voltage	3.135	3.30	3.465	V	
USB_VDD	USB tile DC supply voltage	0.95	1.00	1.05	V	
USB_VDD33	USB peripheral supply	3.135	3.30	3.465	V	
PLL_AVD	PLL analog supply	0.95	1.00	1.05	V	

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
Ta	Ambient operating temperature (Commercial)	0		70	°C	
Tj	Junction temperature			125	°C	

8.3. DC CHARACTERISTICS

Table 13: DC charactersistics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2.00		3.60	V	A
V(IL)	Input low voltage	-0.30		0.70	V	A
V(OH)	Output high voltage	2.20			V	B
V(OL)	Output low voltage			0.40	V	B
I(PU)	Internal pull-up current (Vin=0V)	-100			µA	C
I(PD)	Internal pull-down current (Vin=3.3V)			100	µA	C
I(LC)	Input leakage current	-10		10	µA	

A All pins except power supply pins.

B Measured with 4 mA drivers sourcing 4 mA, 8 mA drivers sourcing 8 mA.

C Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry. In order to pull the pin to the opposite state, a 4K resistor is recommended to overome the internal pull current.

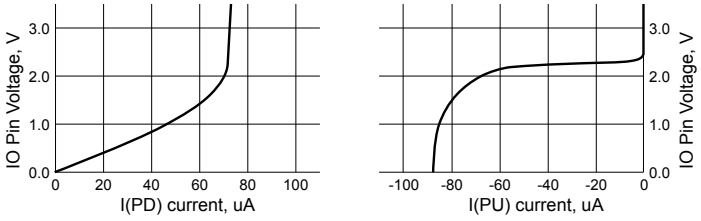


Figure 13: Typical internal pull-down and pull-up currents

8.4. ESD STRESS VOLTAGE

Table 14: ESD stress voltage

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
HBM	Human body model	2.00		2.00	KV	
CDM	Charged device model	-500		500	V	

8.5. RESET TIMING

Table 15: Reset timing

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(RST)	Reset pulse width	5			µs	
T(INIT)	Initialisation time			150	µs	A

A Shows the time taken to start booting after RST_N has gone high

8.6. POWER CONSUMPTION

Table 16: Power consumption

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
I(DDCQ)	Quiescent VDD current		45		mA	A, B, C
PD	Tile power dissipation		325		µW/MIPS	A, D, E, F
IDD	Active VDD current		570	700	mA	A, G
I(ADDPLL)	PLL_AVDD current		5	7	mA	H
I(VDD33)	VDD33 current		53.4		mA	I
I(USB_VDD)	USB_VDD current		16.6		mA	J

A Use for budgetary purposes only.

B Assumes typical tile and I/O voltages with no switching activity.

C Includes PLL current.

D Assumes typical tile and I/O voltages with nominal switching activity.

E Assumes 1MHz = 1 MIPS.

F PD(TYP) value is the usage power consumption under typical operating conditions.

G Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.

H PLL_AVDD = 1.0 V

I HS mode transmitting while driving all 0's data (constant JKJK on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.

J HS receive mode; no traffic.

8.7. CLOCK

Table 17: Clock

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f	Frequency	3.25	24	100	MHz	
SR	Slew rate	0.10			V/ns	
TJ(LT)	Long term jitter (pk-pk)			2	%	A
f(MAX)	Processor clock frequency			500	MHz	b

A Percentage of CLK period.

B Assumes typical tile and I/O voltages with nominal activity

8.8. JTAG TIMING

Table 18: JTAG timing

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
f(TCK_D)	TCK frequency (debug)			18	MHz	
f(TCK_B)	TCK frequency (boundary scan)			10	MHz	
T(SETUP)	TDO to TCK setup time	5			ns	A
T(HOLD)	TDO to TCK hold time	5			ns	A
T(DELAY)	TCK to output delay			15	ns	B

A Timing applies to TMS and TDI inputs.

B Timing applies to TDO output from negative edge of TCK.

9. XVF3510 CHECKLISTS

☑ This section contains checklists for schematics and PCB designers using the XVF3510. Each section contains items to check for a design.

9.1. SCHEMATICS DESIGN CHECK LIST

9.1.1. POWER SUPPLIES

☐ The VDD (core) supply ramps monotonically (rises constantly) from 0V to its final value (0.95V - 1.05V) within 10ms (Section 4.3).

☐ The VDD (core) supply is capable of supplying 1400mA (Section 4.3).

☐ PLL_AVDD is filtered with a low pass filter, for example an RC filter, (Section 4.3)

9.1.2. POWER SUPPLY DECOUPLING

☐ The design has multiple decoupling capacitors per supply, for example less than 12 402 or 0603 size surface mount capacitors of 100nF in value, per supply (Section 4.3).

☐ A bulk decoupling capacitor of at least 10uF is placed on each supply (Section 4.3).

9.1.3. POWER ON RESET

☐ The RST_N pins are asserted (low) until all supplies are good. There is enough time between VDDIO power good and RST_N to allow any boot flash to settle (Section 4.3).

9.1.4. CLOCKS

☐ The CLK input pin is supplied with a clock with monotonic rising edges and low jitter.

☐ A 24MHz reference clock must be connected to the CLK pin.

☐ All clock signals (CLK, MIC_CLK, QSPI_CLK, I2S_CLK) and other audio signal must be routed well following high speed digital design guidelines, and may need buffering.

9.1.5. BOOT

☐ To boot from QSPI flash, QSPI_CS_N, QSPI_D0 .. QSPI_D3, QSPI_D1_BOOTSEL, QSPI_CLK are connected and QSPI_D1_BOOTSEL is connected to QSPI D1 pin on flash device or pulled low/left floating (Section 4.2).

☐ A device specific spispec file is available.

☐ To boot from the local host processor through SPI, QSPI_D1_BOOTSEL must be pulled high and SPI_CS_N, SPI_MOSI and SPI_MISO must be connected.

9.1.6. JTAG AND DEBUGGING

☐ You have decided as to whether you need an XSYS header or not (Section 6)

☐ If you have not included an XSYS header, you have devised a method to program the SPI-flash or OTP (Section 6).

9.2. PCB LAYOUT DESIGN CHECK LIST

9.2.1. GROUND PLANE

- ☐ Multiple vias (eg, 16) have been used to connect the ground to the PCB ground plane. These minimize impedance and conduct heat away from the device. (Section 4.3)
- ☐ Other than ground vias, there are no (or only a few) vias underneath or closely around the device. This creates a good, solid, ground plane.

9.2.2. POWER SUPPLY DECOUPLING

- ☐ The decoupling capacitors are all placed close to a supply pin (Section 4.3).
- ☐ The decoupling capacitors are spaced around the device (Section 4.3).
- ☐ The ground side of each decoupling capacitor has a direct path back to the center ground of the device.

9.2.3. PLL_AVDD

- ☐ The PLL_AVDD filter (especially the capacitor) is placed close to the PLL_AVDD pin (Section 4.3).

10.FURTHER INFORMATION

Title	Download
VocalFusion Dev Kit User Guide	http://www.xmos.com/file/vocalfusion-dev-kit-user-guide
VocalFusion Dev Kit for Amazon AVS User Guide	http://www.xmos.com/file/vocalfusion-dev-kit-for-amazon-avs-user-guide
XMOS Tools User Guide	http://www.xmos.com/file/xmos-tools-user-guide
XVF3510-QF60 Control Guide	http://www.xmos.com/file/xvf3510-qf60-control-guide

11.REVISION HISTORY

Date	Comment
2019-06-12	Early access release