

# xCORE VocalFusion 4-Mic Kit for Amazon AVS Hardware Manual

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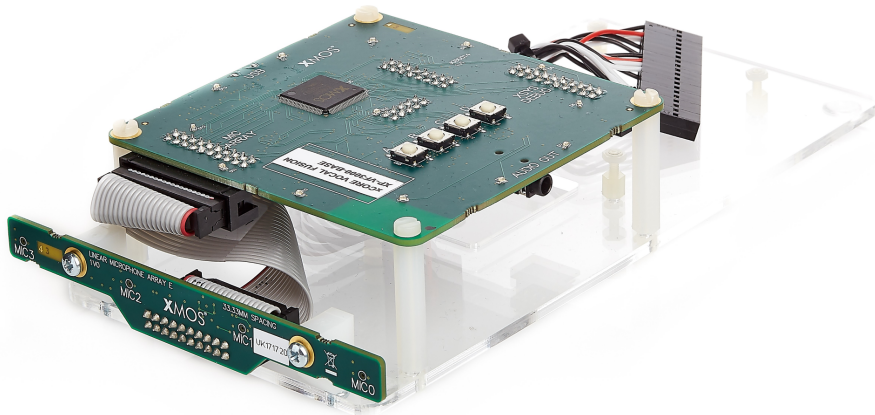
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The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** is an application specific design for far-field voice capture and processing, targetted at Amazon Alexa Voice Service (AVS) applications.

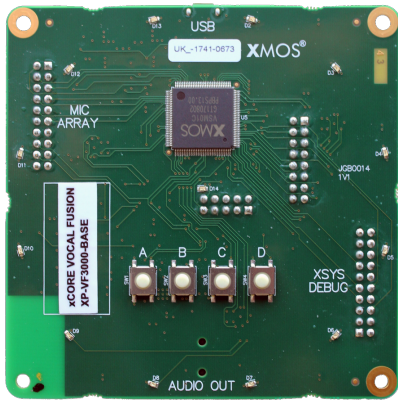
The kit is based on the XMOS XVF3000 voice processor and includes:

- ▶ linear array of 4 omni-directional microphones
- ▶ low-jitter audio clock
- ▶ configurable user input buttons and LEDs
- ▶ I2S audio and I2C control connectivity
- ▶ USB powered, with optional USB2.0 device audio and control connectivity

The XVF3000 on the kit is pre-flashed with a software that implements the xCORE VocalFusion microphone capture and voice processing library, audio and control connectivity, user interfaces and system control.



**Figure 1:**  
xCORE  
VocalFusion  
4-Mic Kit for  
AVS



**Figure 2:**  
xCORE  
VocalFusion  
BaseBoard

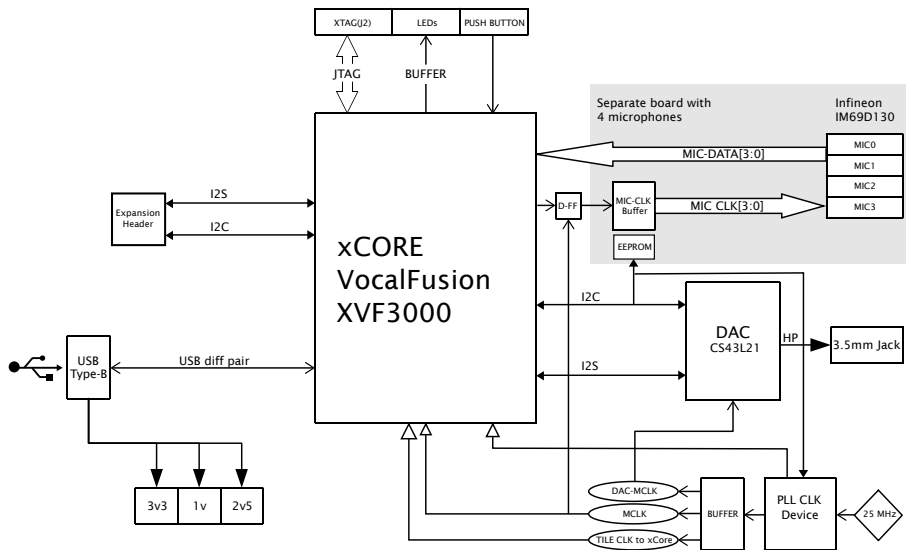


**Figure 3:**  
xCORE  
VocalFusion  
Short Linear  
microphone  
board

# 1 Features

A block diagram for the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** is shown in Figure 4 below. It includes:

- ▶ xCORE VocalFusion XVF3000 voice processor
- ▶ Four MEMS microphones (on a separate board)
- ▶ A micro-USB connector for power (and optionally USB2.0 device connectivity)
- ▶ Extension headers for I2S audio and I2C control connectivity
- ▶ Four general purpose push-button switches
- ▶ 13 user-controlled LEDs
- ▶ Low-jitter audio clock source
- ▶ An xSYS connector for an xTAG debug adapter



**Figure 4:**  
xCORE  
VocalFusion  
4-Mic Kit for  
Amazon AVS  
block  
diagram

## 2 Introduction

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** (XK-VF3000-L33-AVS, Figure 1) consists of an xCORE VocalFusion BaseBoard (XP-VF3000-BASE, Figure 2) and a separate linear microphone array (LINEAR MICROPHONE ARRAY E, Figure 3) using Infineon IM69D130<sup>1</sup> MEMS microphones.

The VocalFusion BaseBoard is based on the XMOS XVF3000 device, running a software which integrates the xCORE VocalFusion microphone capture and voice processing library to provide: beamforming, acoustic echo cancellation, noise suppression, de-reverberation and automatic gain control.

The XVF3000 device has 16 32-bit logical processing cores and integrates 2MBytes Quad Serial Peripheral Interface (QSPI) flash in a TQ128 package.

For general information on the XVF3000 device see the xCORE-200 Architecture Overview<sup>2</sup>. For device specific information on the XVF3000 device see the XVF3000 Datasheet<sup>3</sup>.

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<sup>1</sup><http://www.infineon.com/microphones>

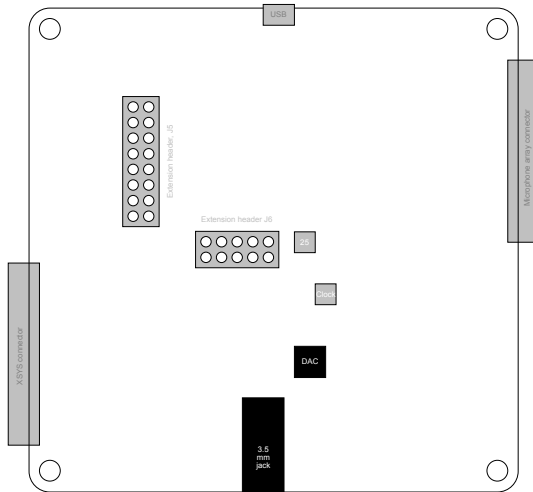
<sup>2</sup><http://www.xmos.com/published/xcore-architecture>

<sup>3</sup>[http://www.xmos.com/published/xvf3000\\_3100-tq128-datasheet](http://www.xmos.com/published/xvf3000_3100-tq128-datasheet)



## 4 Stereo DAC with headphone amplifier

A CS43L21 stereo DAC with integrated headphone amplifier is used to generate audio output on a 3.5mm audio jack. The CS43L21 is connected to the XVF3000 device through an I2S interface and is configured using the I2C bus (see §6, below).



**Figure 6:**  
DAC and  
3.5mm audio  
jack locations

The I2S interface of the CS43L21 stereo DAC/HPA is connected to the XVF3000 GPIO pins as shown in Figure 7.

GPIO pin	Port	Signal
X1D28	P4F0	DAC_RST_N
X1D36	P1M0	I2S_BCLK
X1D37	P1N0	I2S_LRCK
X1D38	P1O0	MCLK_TILE1
X1D39	P1P0	I2S_DAC_DATA

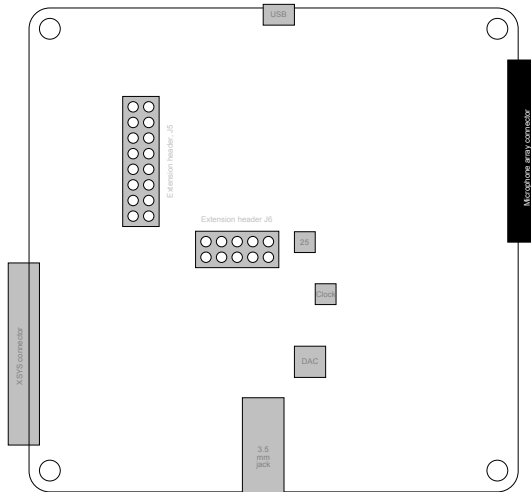
**Figure 7:**  
Stereo DAC  
GPIO pins

## 5 MEMS microphone board

The microphone board is plugged into connector J3 on the BaseBoard using a ribbon cable. A short ribbon cable should be used for signal integrity.



The microphones should **not** be plugged into the xSYS connector.



**Figure 8:**  
Microphone  
connector  
location

The microphone array consists of a linear array of four microphones (spaced 33mm apart), a clock buffer, voltage level shifters and an EEPROM for optional identification.

The microphone signals are connected to the XVF3000 GPIO pins as shown in Figure 9.

Microphone	GPIO pin	Port
MIC_CLK	X0D12	P1E0
MCLK_IN	X0D13	P1F0
MIC_0	X0D14	P8B0
MIC_1	X0D15	P8B1
MIC_2	X0D16	P8B2
MIC_3	X0D17	P8B3

**Figure 9:**  
Linear MEMS  
microphone  
board GPIO  
pins

## 6 I2C bus

The BaseBoard has a main I2C bus that is used to control the DAC, clock generator, and EEPROM. This main I2C bus is connected to tile 1 of the XVF3000, with the XVF3000 acting as a master on this I2C bus. See Figure 10 below.

**Figure 10:**  
I2C master  
GPIO pins

GPIO pin	Port	Signal
X1D26	P4E0	I2C_SCL
X1D27	P4E1	I2C_SDA

The addresses of devices on the I2C bus are shown in Figure 11 below.

**Figure 11:**  
I2C device  
addresses

Device	Address
Si5351A (Clock)	0b1100010 0x62
CS43L21 (DAC)	0b1001010 0x4A
24LC08B (EEPROM on microphone board)	0b1010Xxx 0x5x

Please refer to the 24LC08B datasheet for details on how to set the address of the EEPROM.

The BaseBoard also has a secondary I2C bus, on which the XVF3000 is a slave - so allowing the XVF3000 to be controlled by an external I2C host. See Figure 12 below.

**Figure 12:**  
I2C slave  
GPIO pins

GPIO pin	Port	Signal
X0D24	P1I0	I2C_SDA_SLAVE
X0D25	P1J1	I2C_SCL_SLAVE

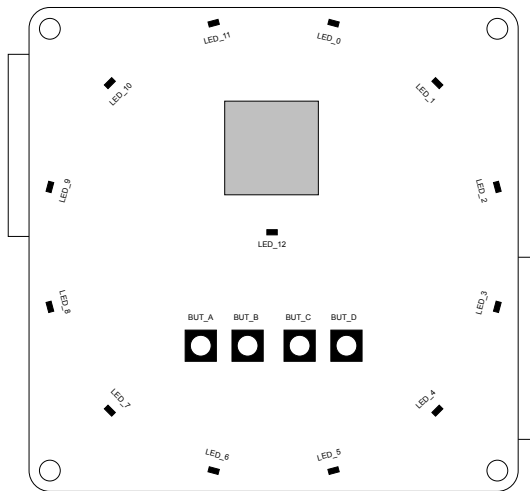
This slave I2C interface is wired up to the extension headers (see §8).



## 7 General purpose user interface

The BaseBoard has 13 LEDs that are controlled by the XVF3000 GPIO. LED\_0 - LED\_11 (D2-D13) are positioned around the edge of the BaseBoard. LED\_12 (D14) is positioned in the middle of the BaseBoard. The LED GPIO output must be set low to light the corresponding LED.

Four general purpose push-button switches are provided. When pressed, each button creates a connection from the I/O to GND. To ensure correct behavior, the port connected to the buttons (P4A) must always be defined as an input.



**Figure 13:**  
General purpose user interface component locations

The signal mapping of the user interface components to the XVF3000 GPIO is shown in Figure 14 and Figure 15.

UI signal	GPIO pin	Port
BUTTON_A	X0D02	P4A0
BUTTON_B	X0D03	P4A1
BUTTON_C	X0D08	P4A2
BUTTON_D	X0D09	P4A3

**Figure 14:**  
User interface GPIO pins

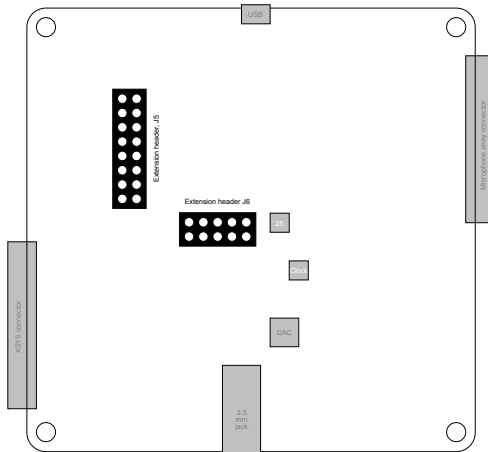
UI signal	GPIO pins	Port
LED_0	X0D26	P16B0
LED_1	X0D27	P16B1
LED_2	X0D28	P16B2
LED_3	X0D29	P16B3
LED_4	X0D30	P16B4
LED_5	X0D31	P16B5
LED_6	X0D32	P16B6
LED_7	X0D33	P16B7
LED_8	X0D34	P1K0
LED_9	X0D35	P1L0
LED_10	X0D36	P16B8
LED_11	X0D37	P16B9
LED_12	X0D38	P16B10

**Figure 15:**  
User interface  
GPIO pins

A green LED (PGOOD) near the USB connector indicates 3V3 and 1V0 supplies are up.

## 8 Extension headers

The BaseBoard has a two extension headers, J5 and J6, containing: digital audio signals, the secondary I2C bus (see §6) and several general purpose IOs controlled by the XVF3000.



**Figure 16:**  
Extension  
header  
locations

These signals allow the XVF3000 to be connected to and controlled by an external applications processor host.

The software pre-flashed<sup>4</sup> in to the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** configures the XVF3000 device and the BaseBoard hardware to use these extension headers to connect to an external applications processor host.

- ▶ Audio input/output connectivity via I2S signals available on J6.  
The XVF3000 is the I2S master.
- ▶ Control via I2C signals available on J5.  
The XVF3000 is an I2C slave.

The signal mapping of the extension headers to the XVF3000 GPIO is shown in Figure 17 and Figure 18.

<sup>4</sup>VocalFusion software build configuration: i10o0\_lin33\_i2s\_only\_master\_48kHz\_i2cct1

Pin	GPIO pin	Port	Signal	Notes
1	X0D22	P1G0		<i>Not used</i>
2			GND	Ground
3	X0D23	P1H0		<i>Not used</i>
4	X1D35	P1L0		<i>Not used</i>
5	X0D00	P1A0		<i>Not used</i>
6			GND	Ground
7	X0D11	P1D0		<i>Not used</i>
8			GND	Ground
9	X0D24	P1I0	I2C_SDA_SLAVE	Add a pull-up resistor
10	X0D39	P1P0		<i>Not used</i>
11			GND	Ground
12	X0D25	P1J0	I2C_SCL_SLAVE	Add a pull-up resistor
13			3V3	3.3V from BaseBoard
14			GND	Ground
15			EXT_MCLK	MCLK input (not used)
16			GND	Ground

**Figure 17:**  
Extension  
header J5  
GPIO pins  
(XVF3000 an  
I2C slave)

Pin	GPIO pin	Port	Signal	Notes
1	X1D37	P1N0	I2S_LRCK	I2S LRCLK from XVF3000 to host
2			GND	Ground
3	X1D39	P1P0	I2S_DAC_DATA	I2S data from host to XVF3000 and DAC
4			NC	<i>No connection</i>
5			GND	Ground
6	X1D36	P1M0	I2S_BCLK	I2S BCLK from XVF3000 to host
7	X1D38	P1O0	MCLK_TILE1	MCLK output to host
8			GND	Ground
9	X1D11	P1D0	X1D11	I2S data from XVF3000 to host
10	X1D10	P1C0	X1D10	<i>Not used</i>

**Figure 18:**  
Extension  
header J6  
GPIO pins  
(XVF3000 the  
I2S master)

The XVF3000 device and BaseBoard hardware *can* support other modes of audio and control connectivity. Some of these other modes are mentioned below for example only - their use requires a different XVF3000 software.

**XVF3000 as the I2S master** (default software, as described above)

- ▶ Example VocalFusion build configuration: `1i0o0_lin33_i2s_only_master_48kHz_i2cctl`
- ▶ Audio input/output via I2S signals on J6. The XVF3000 is the I2S master.
- ▶ Control via I2C on J5. The XVF3000 is an I2C slave.
- ▶ Extension headers are mapped to the XVF3000 GPIO as shown in Figure 17 and Figure 18 above.

**XVF3000 as an I2S slave**

To use this mode, remove R67 and insert a 0R link into R17.

- ▶ Example VocalFusion build configuration: `1i0o0_lin33_i2s_only_48kHz_i2cctl`
- ▶ Audio input/output via I2S on J6. The XVF3000 is an I2S slave.
- ▶ Control via I2C on J5. The XVF3000 is an I2C slave.
- ▶ 24.576 MHz MasterClock generated externally and connected to J5 pin 15.
- ▶ Extension headers mapped to the XVF3000 GPIO as shown in Figure 17 above and Figure 19 below.

J6 pin	GPIO pins	Port	Signal	Notes
1	X1D37	P1N0	I2S_LRCK	I2S LRCLK from host to XVF3000
2			GND	Ground
3	X1D39	P1P0	I2S_DAC_DATA	I2S data from host to DAC
4			NC	<i>No connection</i>
5			GND	Ground
6	X1D36	P1M0	I2S_BCLK	I2S BLCK from host to XVF3000
7	X1D38	P1O0	MCLK_TILE1	MCLK output (not used)
8			GND	Ground
9	X1D11	P1D0	X1D11	I2S data from XVF3000 to host
10	X1D10	P1C0	X1D10	I2S data from host to XVF3000

**Figure 19:**  
Extension header J6 GPIO pins (XVF3000 as I2S slave)

**XVF3000 as an USB 2.0 device**

If using this mode, both extension headers should be left unconnected.

- ▶ Example VocalFusion build configuration: `1i1o2_lin33`
- ▶ Audio input/output via USB. The XVF3000 is a USB Audio Class 1 device.
- ▶ Control via USB. The XVF3000 is a custom class control device.

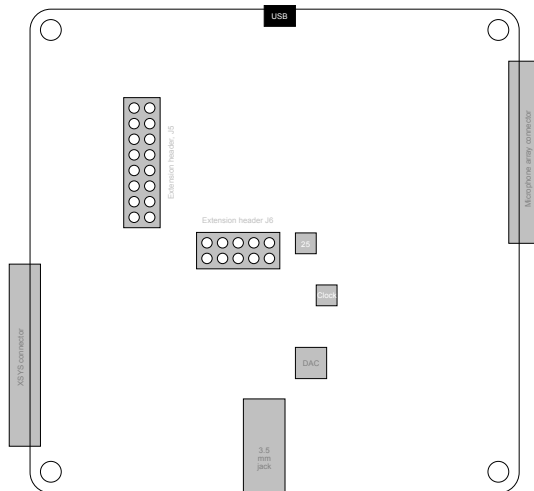
## 9 USB port

The USB micro-B port (J1) provides power for all the on-board circuits and is used to generate the following voltage rails:

- ▶ +1V0 (Core voltage to XMOS device)
- ▶ +2V5 (for headphone amplifier in DAC device)
- ▶ +3V3 for GPIOs and other accessory devices

Voltage tolerance should be as per USB VBUS specification values.

Proper power-on sequence is indicated by power good LED (D1) in bottom side of the board.



**Figure 20:**  
USB  
components

The data lines from the USB micro-B port (J1) are connected to the XVF3000's integrated USB PHY, and so (with a different XVF3000 software) *can* be used to provide USB audio and/or control connectivity to the XVF3000 and the BaseBoard.

**Note:**

- ▶ the software pre-flashed in to the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** does **not** provide any USB connectivity.
- ▶ J1 must be connected at all times to provide power to the BaseBoard, even though the USB interface is not used.

## 10 Flash memory

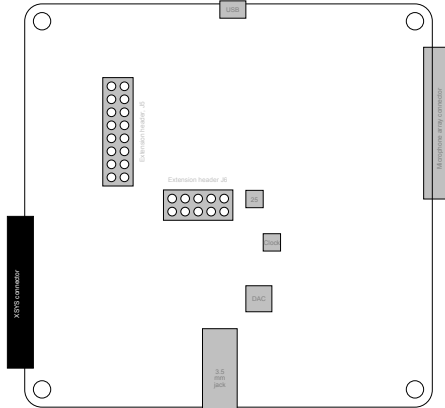
The XVF3000 device includes 2MBytes of QSPI flash memory, which is internally interfaced to the XVF3000 by the GPIO connections shown in Figure 21:

QSPI signal	GPIO pin	Port
QSPI_SS	X0D01	P1B
QSP_D0	X0D04	P4B0
QSP_D1	X0D05	P4B1
QSP_D2	X0D06	P4B2
QSP_D3	X0D07	P4B3
SPI_CLK	X0D10	P1C

**Figure 21:**  
QSPI Flash  
GPIO pins

## 11 xSYS connector

A standard XMOS xSYS interface (J2) is provided. The can connect to an XMOS xTAG debug adaptor, allowing host debug of the board via JTAG.



**Figure 22:**  
xSYS  
connector

xSYS signal	GPIO pin	Header pin	Description
TMS	See note	7	JTAG Test Mode Select
TCK	See note	9	JTAG Test Clock
TDI	See note	5	JTAG Test Data In - from debug adapter to xCORE
TDO	See note	13	JTAG Test Data Out - from xCORE to debug adapter
RST_N	See note	15	System Reset - active low, resets xCORE device
GND		4, 8, 12, 16, 20	Ground
XL_UP1	X0D43	6	XMOS link, uplink bit 1
XL_UP0	X0D42	10	XMOS link, uplink bit 0
XL_DN0	X0D40	14	XMOS link, downlink bit 0
XL_DN1	X0D41	18	XMOS link, downlink bit 1

**Figure 23:**  
xSYS  
Connector  
Pinout

Notes:

- ▶ JTAG connections occupy dedicated connections



## 12 xCORE VocalFusion BaseBoard portmap

The tables below detail the port-pin mappings for the xCORE VocalFusion BaseBoard, as programmed with the default software.

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X0D00	1A <sup>0</sup>					
X0D01	1B <sup>0</sup>					QSPI_CS
X0D02		4A <sup>0</sup>	8A <sup>0</sup>	16A <sup>0</sup>	32A <sup>20</sup>	BUTTON_A
X0D03		4A <sup>1</sup>	8A <sup>1</sup>	16A <sup>1</sup>	32A <sup>21</sup>	BUTTON_B
X0D04		4B <sup>0</sup>	8A <sup>2</sup>	16A <sup>2</sup>	32A <sup>22</sup>	QSPI_D0
X0D05		4B <sup>1</sup>	8A <sup>3</sup>	16A <sup>3</sup>	32A <sup>23</sup>	QSPI_D1
X0D06		4B <sup>2</sup>	8A <sup>4</sup>	16A <sup>4</sup>	32A <sup>24</sup>	QSPI_D2
X0D07		4B <sup>3</sup>	8A <sup>5</sup>	16A <sup>5</sup>	32A <sup>25</sup>	QSPI_D3
X0D08		4A <sup>2</sup>	8A <sup>6</sup>	16A <sup>6</sup>	32A <sup>26</sup>	BUTTON_C
X0D09		4A <sup>3</sup>	8A <sup>7</sup>	16A <sup>7</sup>	32A <sup>27</sup>	BUTTON_D
X0D10	1C <sup>0</sup>					QSPI_CLK
X0D11	1D <sup>0</sup>					
X0D12	1E <sup>0</sup>					MIC_CLK
X0D13	1F <sup>0</sup>					MCLK_IN
X0D14		4C <sup>0</sup>	8B <sup>0</sup>	16A <sup>8</sup>	32A <sup>28</sup>	MIC_0
X0D15		4C <sup>1</sup>	8B <sup>1</sup>	16A <sup>9</sup>	32A <sup>29</sup>	MIC_1
X0D16		4D <sup>0</sup>	8B <sup>2</sup>	16A <sup>10</sup>		MIC_2
X0D17		4D <sup>1</sup>	8B <sup>3</sup>	16A <sup>11</sup>		MIC_3
X0D18		4D <sup>2</sup>	8B <sup>4</sup>	16A <sup>12</sup>		MIC_4
X0D19		4D <sup>3</sup>	8B <sup>5</sup>	16A <sup>13</sup>		MIC_5
X0D20		4C <sup>2</sup>	8B <sup>6</sup>	16A <sup>14</sup>	32A <sup>30</sup>	MIC_6
X0D21		4C <sup>3</sup>	8B <sup>7</sup>	16A <sup>15</sup>	32A <sup>31</sup>	MIC_7
X0D22	1G <sup>0</sup>					
X0D23	1H <sup>0</sup>					
X0D24	1I <sup>0</sup>					I2C_SDA_SLAVE
X0D25	1J <sup>0</sup>					I2C_SCL_SLAVE
X0D26		4E <sup>0</sup>	8C <sup>0</sup>	16B <sup>0</sup>		LED_0
X0D27		4E <sup>1</sup>	8C <sup>1</sup>	16B <sup>1</sup>		LED_1
X0D28		4F <sup>0</sup>	8C <sup>2</sup>	16B <sup>2</sup>		LED_2
X0D29		4F <sup>1</sup>	8C <sup>3</sup>	16B <sup>3</sup>		LED_3
X0D30		4F <sup>2</sup>	8C <sup>4</sup>	16B <sup>4</sup>		LED_4
X0D31		4F <sup>3</sup>	8C <sup>5</sup>	16B <sup>5</sup>		LED_5
X0D32		4E <sup>2</sup>	8C <sup>6</sup>	16B <sup>6</sup>		LED_6
X0D33		4E <sup>3</sup>	8C <sup>7</sup>	16B <sup>7</sup>		LED_7
X0D34	1K <sup>0</sup>					LED_8
X0D35	1L <sup>0</sup>					LED_9
X0D36	1M <sup>0</sup>		8D <sup>0</sup>	16B <sup>8</sup>		LED_10
X0D37	1N <sup>0</sup>		8D <sup>1</sup>	16B <sup>9</sup>		LED_11
X0D38	1O <sup>0</sup>		8D <sup>2</sup>	16B <sup>10</sup>		LED_12
X0D39	1P <sup>0</sup>		8D <sup>3</sup>	16B <sup>11</sup>		
X0D40			8D <sup>4</sup>	16B <sup>12</sup>		XL_DN1
X0D41			8D <sup>5</sup>	16B <sup>13</sup>		XL_DN0
X0D42			8D <sup>6</sup>	16B <sup>14</sup>		XL_UP0
X0D43			8D <sup>7</sup>	16B <sup>15</sup>		XL_UP1

**Figure 24:**  
 xCORE  
 VocalFusion  
 BaseBoard  
 Portmap:  
 Tile0

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X1D00	1A <sup>0</sup>					
X1D01	1B <sup>0</sup>					
X1D02		4A <sup>0</sup>	8A <sup>0</sup>	16A <sup>0</sup>	32A <sup>20</sup>	
X1D03		4A <sup>1</sup>	8A <sup>1</sup>	16A <sup>1</sup>	32A <sup>21</sup>	
X1D04		4B <sup>0</sup>	8A <sup>2</sup>	16A <sup>2</sup>	32A <sup>22</sup>	
X1D05		4B <sup>1</sup>	8A <sup>3</sup>	16A <sup>3</sup>	32A <sup>23</sup>	
X1D06		4B <sup>2</sup>	8A <sup>4</sup>	16A <sup>4</sup>	32A <sup>24</sup>	
X1D07		4B <sup>3</sup>	8A <sup>5</sup>	16A <sup>5</sup>	32A <sup>25</sup>	
X1D08		4A <sup>2</sup>	8A <sup>6</sup>	16A <sup>6</sup>	32A <sup>26</sup>	
X1D09		4A <sup>3</sup>	8A <sup>7</sup>	16A <sup>7</sup>	32A <sup>27</sup>	
X1D10	1C <sup>0</sup>					
X1D11	1D <sup>0</sup>					I2S_VOICE_DATA*
X1D14		4C <sup>0</sup>	8B <sup>0</sup>	16A <sup>8</sup>	32A <sup>28</sup>	
X1D15		4C <sup>1</sup>	8B <sup>1</sup>	16A <sup>9</sup>	32A <sup>29</sup>	
X1D16		4D <sup>0</sup>	8B <sup>2</sup>	16A <sup>10</sup>		
X1D17		4D <sup>1</sup>	8B <sup>3</sup>	16A <sup>11</sup>		
X1D18		4D <sup>2</sup>	8B <sup>4</sup>	16A <sup>12</sup>		
X1D19		4D <sup>3</sup>	8B <sup>5</sup>	16A <sup>13</sup>		
X1D20		4C <sup>2</sup>	8B <sup>6</sup>	16A <sup>14</sup>	32A <sup>30</sup>	
X1D21		4C <sup>3</sup>	8B <sup>7</sup>	16A <sup>15</sup>	32A <sup>31</sup>	
X1D26		4E <sup>0</sup>	8C <sup>0</sup>	16B <sup>0</sup>		I2S_SCL
X1D27		4E <sup>1</sup>	8C <sup>1</sup>	16B <sup>1</sup>		I2S_SDA
X1D28		4F <sup>0</sup>	8C <sup>2</sup>	16B <sup>2</sup>		DAC_RST_N
X1D29		4F <sup>1</sup>	8C <sup>3</sup>	16B <sup>3</sup>		
X1D30		4F <sup>2</sup>	8C <sup>4</sup>	16B <sup>4</sup>		
X1D31		4F <sup>3</sup>	8C <sup>5</sup>	16B <sup>5</sup>		
X1D32		4E <sup>2</sup>	8C <sup>6</sup>	16B <sup>6</sup>		
X1D33		4E <sup>3</sup>	8C <sup>7</sup>	16B <sup>7</sup>		
X1D35	1L <sup>0</sup>					
X1D36	1M <sup>0</sup>		8D <sup>0</sup>	16B <sup>8</sup>		I2S_BCLK
X1D37	1N <sup>0</sup>		8D <sup>1</sup>	16B <sup>9</sup>		I2S_LRCK
X1D38	1O <sup>0</sup>		8D <sup>2</sup>	16B <sup>10</sup>		MCLK_TILE1
X1D39	1P <sup>0</sup>		8D <sup>3</sup>	16B <sup>11</sup>		I2S_PLAYBACK_DATA*
X1D40			8D <sup>4</sup>	16B <sup>12</sup>		
X1D41			8D <sup>5</sup>	16B <sup>13</sup>		
X1D42			8D <sup>6</sup>	16B <sup>14</sup>		
X1D43			8D <sup>7</sup>	16B <sup>15</sup>		

**Figure 25:**  
 xCORE  
 VocalFusion  
 BaseBoard  
 Portmap:  
 Tile1

Notes\*:

- ▶ Pin X1D11 is the I2S data pin for the captured voice audio from the XVF3000 to the host. The hardware schematic labels this signal X1D11. The VocalFusion software calls this port I2S\_DAC, because it is an output from the software.

- ▶ Pin X1D39 is the I2S data pin for the playback audio from the host to the XVF3000 and the DAC. The hardware schematic labels this signal I2S\_DAC\_DATA. The VocalFusion software calls this port I2S\_ADC, because it is an input to the software.

## 13 Raspberry Pi interface cable

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** is supplied with a cable to interface the BaseBoard (via J5 and J6 - see §8) to a Raspberry Pi.

The interface cable makes the connections as shown in the table below.

Raspberry Pi Signal	J8	cable color	J5	J6	BaseBoard Signal	XVF3000 Pin	XVF3000 Port	Notes
SDA	3	white	9		X0D24	X0D24	P1I0	I2C SDA between Pi (master) and XVF3000 (slave)
SCL	5	white	12		X0D25	X0D25	P1J0	I2C SCL between Pi (master) and XVF3000 (slave)
GND	6	black		2	GND			Ground
GND	9	black		5	GND			Ground
I2S_BCLK	12	white		6	I2S_BCLK	X1D35	P1M0	I2S BCLK from XVF3000 to Pi
GND	14	black		8	GND			Ground
SPL_MOSI	19	white	7		X0D11	X0D11	P1D0	<i>not used</i>
GND	20	black		2	GND			Ground
SPL_MISO	21	white	5		X0D00	X0D00	P1A0	<i>not used</i>
SPL_SCLK	23	red	1		X0D22	X0D22	P1G0	<i>not used</i>
SPL_CEO	24	white	3		X0D23	X0D23	P1H0	<i>not used</i>
GND	25	black	6		GND			Ground
GND	30	black	8		GND			Ground
GND	34	black	11		GND			Ground
I2S_LRCLK	35	red		1	I2S_BCLK	X1D37	P1N0	I2S LRCLK from XVF3000 to Pi
I2S_DIN	38	white		9	X1D11	X1D11	P1D0	I2S data from XVF3000 to Pi
GND	39	black	14		GND			Ground
I2S_DOUT	40	white	3		I2S_DAC_DATA	X1D39	P1P0	I2S data from Pi to XVF3000 and DAC

**Figure 26:**  
Raspberry Pi  
interface  
cable

For more details on how to connect and setup a Raspberry Pi, see:

- ▶ <http://www.xmos.com/vocalfusion-avs>

## 14 Operating requirements

A USB 2.0 high-speed compliant cable of less than 3m in length should be used when operating the **xCORE VocalFusion 4-Mic Kit for Amazon AVS**. XMOS cannot guarantee correct operation of the base board should any other cable be used.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** with appropriate ESD precautions in place.

## 15 Dimensions

The BaseBoard is 90x90mm square with a board thickness of 1.6mm.

## 16 RoHS and REACH

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.



## 17 Schematics

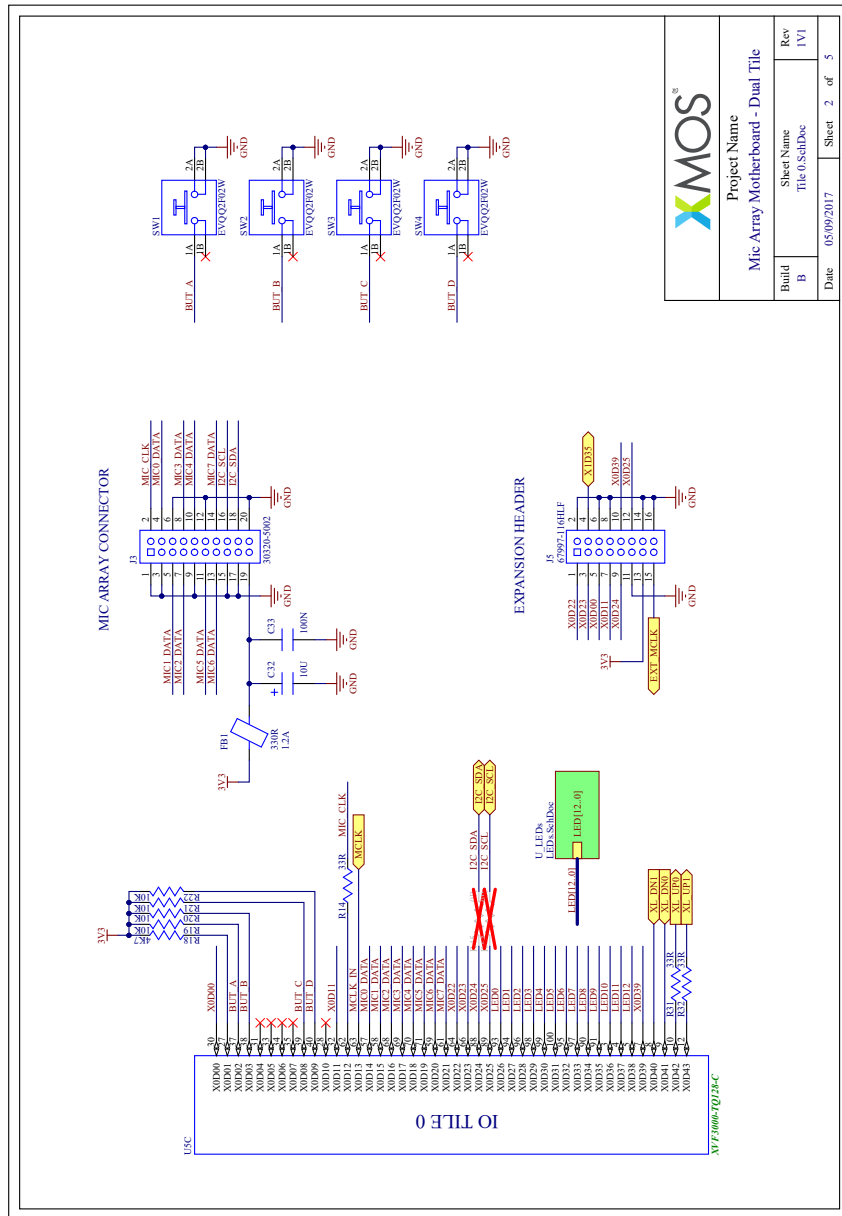
The schematics for the Base Board included in the kit, are shown in the first five figures below, followed by the schematics for the linear array board.

For full reference schematics please contact XMOS:

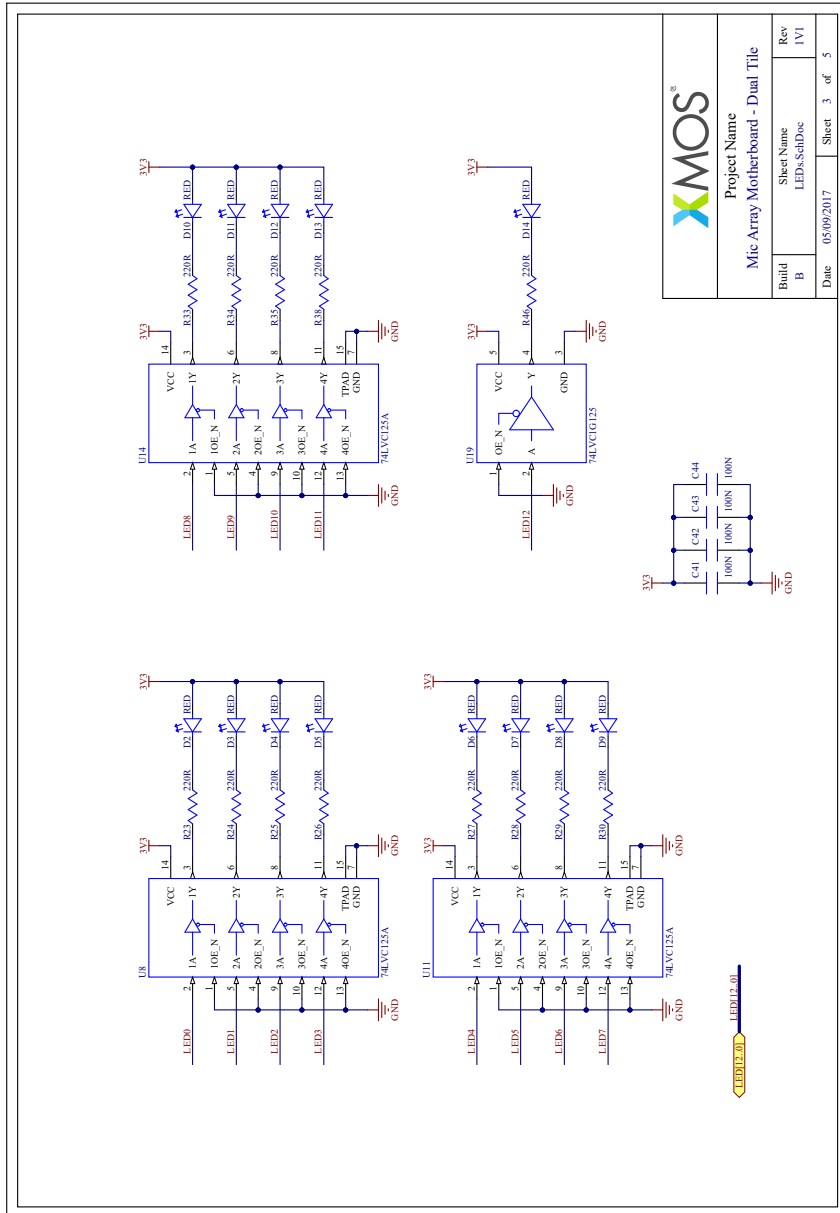
► <https://www.xmos.com/contact/enquiries>



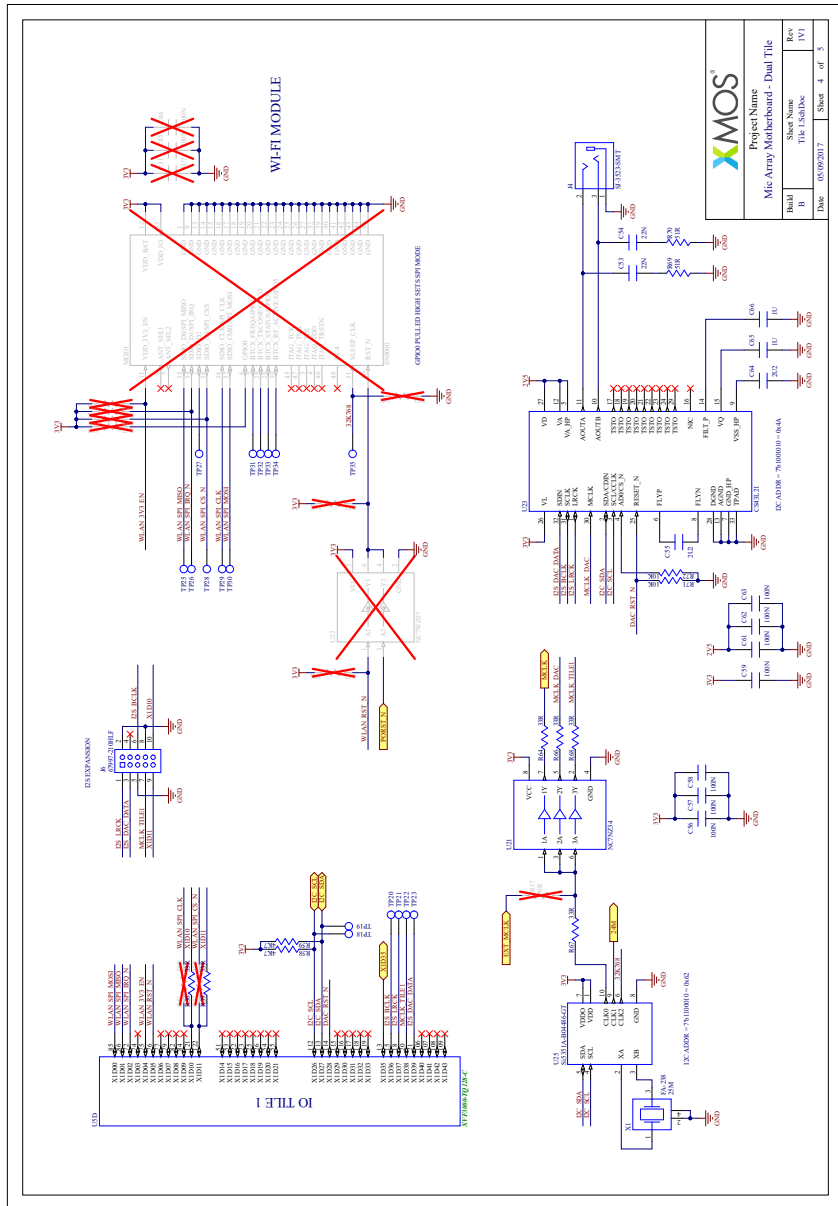
**Figure 28:**  
xCORE  
VocalFusion  
BaseBoard -  
extension  
header,  
buttons,  
Microphone  
header, Tile 0  
IO



**Figure 29:**  
xCORE  
VocalFusion  
BaseBoard -  
LEDs

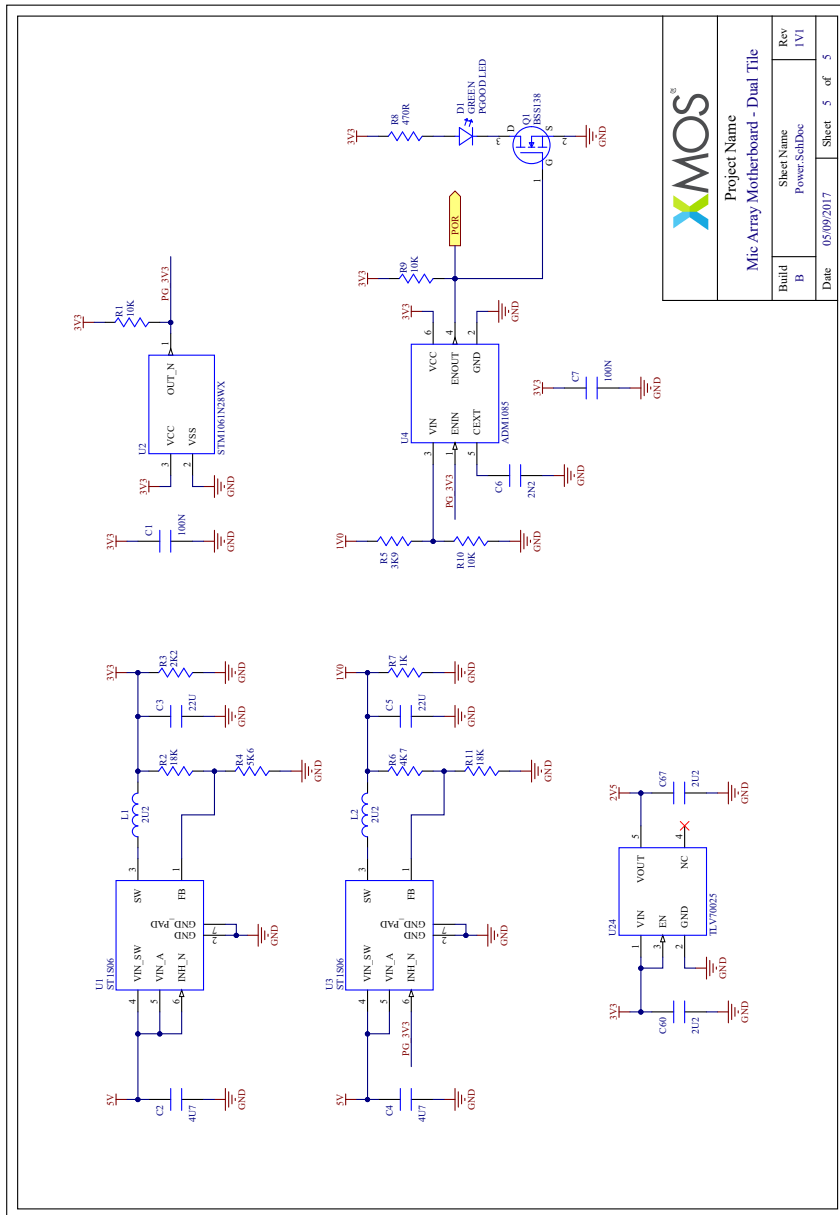



**Figure 30:**  
 xCORE  
 VocalFusion  
 BaseBoard -  
 Clock and  
 stereo DAC  
 with  
 headphone  
 jack circuitry,  
 tile 1 IO

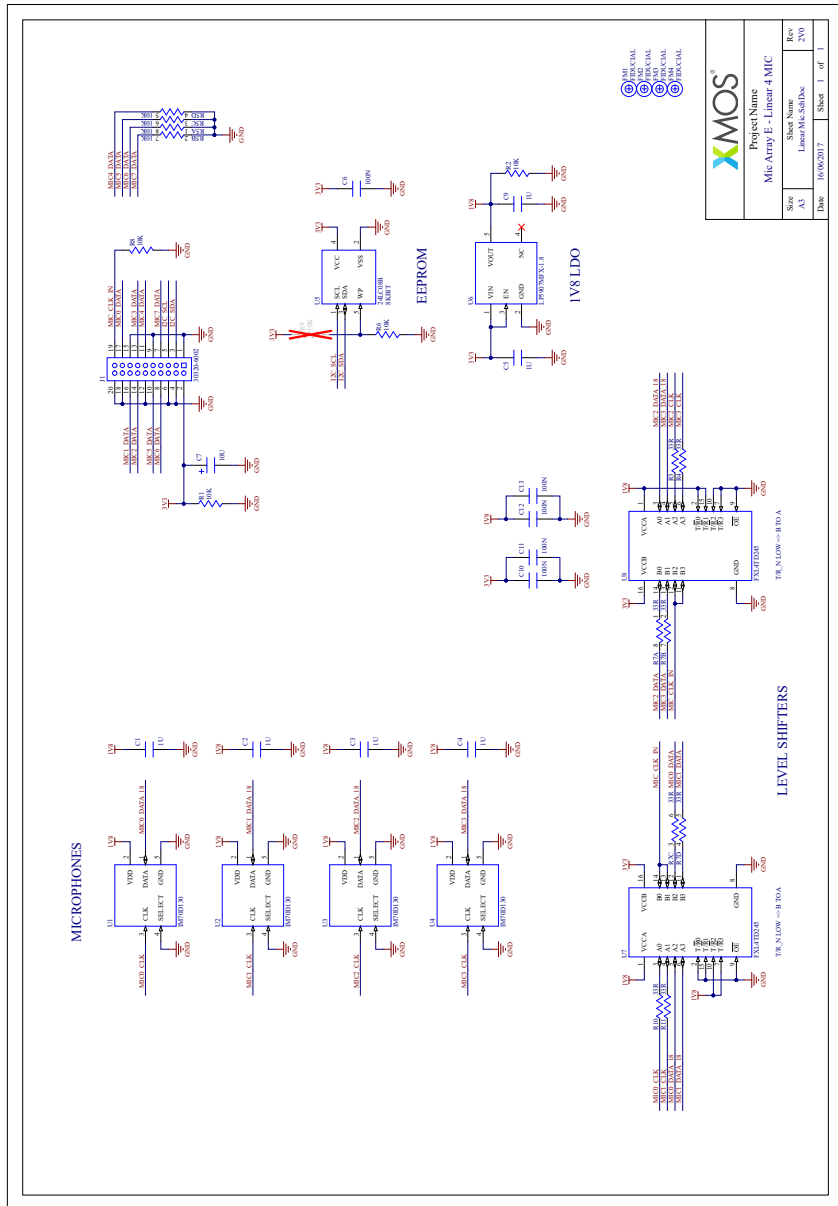




**Figure 31:**  
xCORE  
VocalFusion  
BaseBoard -  
voltage rail  
LDOs and  
reset circuit



		Project Name	
		Mic Array Motherboard - Dual Tile	
Build	Sheet Name	Rev	
	B	Power-SahDee	1V1
Date	05/09/2017	Sheet	5 of 5



**Figure 32:**  
xCORE  
VocalFusion -  
Linear  
Microphone  
Board



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