xCORE VocalFusion 4-Mic Kit for Amazon AVS Hardware Manual

IN THIS DOCUMENT

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** is an application specific design targeted at far-field voice capture and processing for Amazon Alexa Voice Service (AVS) applications.

The kit is based on the XMOS XVF3000 voice processor and integrates the xCORE microphone capture and voice processing library with all the necessary hardware building blocks including:

- linear array of 4 omni-directional microphones
- low-jitter audio clock
- configurable user input buttons and LEDs
- I2S audio and I2C control connectivity
- optional USB2.0 device audio and control connectivity

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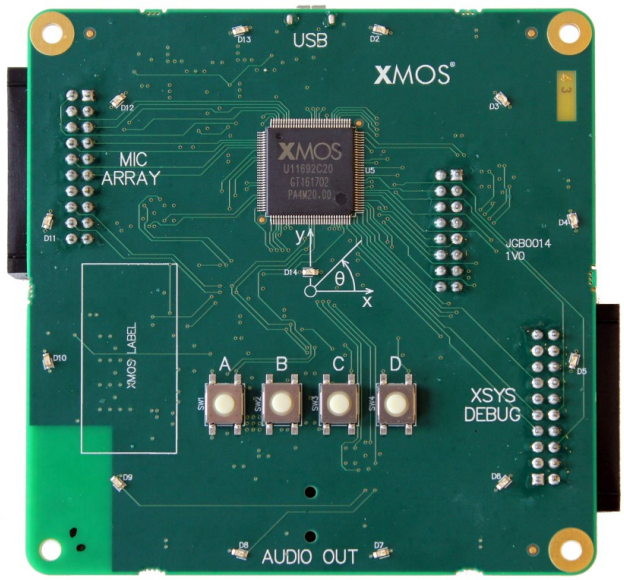

Figure 1: xCORE VocalFusion BaseBoard

Figure 2: xCORE VocalFusion Short Linear microphone board

1 Features

A block diagram for the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** is shown in Figure 3 below. It includes:

- xCORE VocalFusion XVF3000 voice processor
- Four MEMS microphones (on a separate board)
- A micro-USB connector for power (and optionally USB2.0 device connectivity)
- An extension header for I2S audio and I2C control connectivity
- Four general purpose push-button switches (not currently used)
- 13 user-controlled LEDs (not currently used)
- Low-jitter audio clock source
- An xSYS connector for an xTAG debug adapter

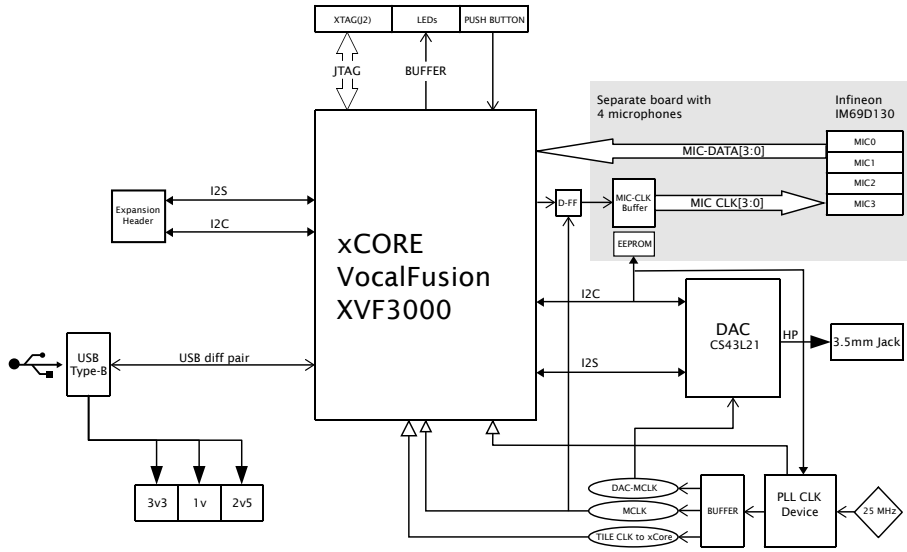

Figure 3: xCORE VocalFusion 4-Mic Kit for Amazon AVS block diagram

2 Introduction

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** (XK-VF3000-L33-AVS) consists of an xCORE VocalFusion BaseBoard (XP-VF3000-BASE, Figure 1) and a separate linear microphone array (LINEAR MICROPHONE ARRAY E, Figure 2) using Infineon IM69D130[1] MEMS microphones.

The VocalFusion BaseBoard is based on the XMOS XVF3000 device, running a software which integrates the xCORE microphone capture and voice processing library to provide: beamforming, acoustic echo cancellation, noise suppression, de-reverberation and automatic gain control.

The XVF3000 device has 16 32-bit logical processing cores and integrates 2MBytes Quad Serial Peripheral Interface (QSPI) flash in a TQ128 package.

For general information on the XVF3000 device see the xCORE-200 Architecture Overview[2]. For device specific information on the XVF3000 device see the XVF3000 Datasheet[3].

[1] http://www.infineon.com/microphones
[2] http://www.xmos.com/published/xcore-architecture
[3] http://www.xmos.com/published/xvf3000_3100-tq128-datasheet

3 Clock sources and distribution

The BaseBoard includes a single clock generator (Si5351A-B04486-GT, U25) that generates two clocks:

- XVF3000 reference clock - 24MHz oscillator
- Low jitter master audio clock - 24.576MHz oscillator, used for the DAC and (indirectly) the microphones

The clock generator is controlled over the I2C bus (see §6, below).

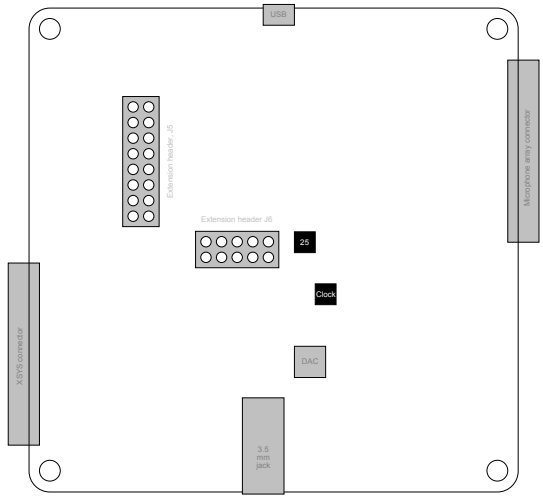

Figure 4: Clock and oscillator locations

4 Stereo DAC with headphone amplifier

A CS43L21 stereo DAC with integrated headphone amplifier is used to generate audio output on a 3.5mm audio jack. The CS43L21 is connected to the XVF3000 device through an I2S interface and is configured using the I2C bus (see §6, below).

The CS43L21 stereo DAC/HPA device is connected to the following pins for its I2S interface:

Pin	Port	Signal
X1D28	P4F0	DAC_RST_N
X1D36	P1M0	I2S_BCLK
X1D37	P1N0	I2S_LRCK
X1D38	P1O0	MCLK_TILE1
X1D39	P1P0	I2S_DAC_DATA

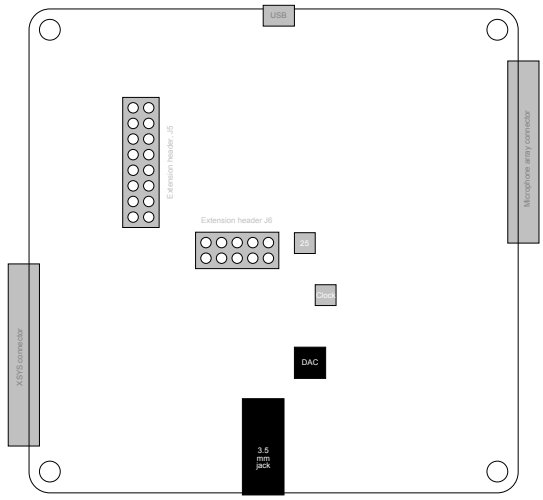

Figure 5: DAC and 3.5mm audio jack locations

5 MEMS microphone board

The microphone board is plugged into connector J3 on the BaseBoard using a ribbon cable. A short ribbon cable should be used for signal integrity.

The microphones should **not** be plugged into the xSYS connector.

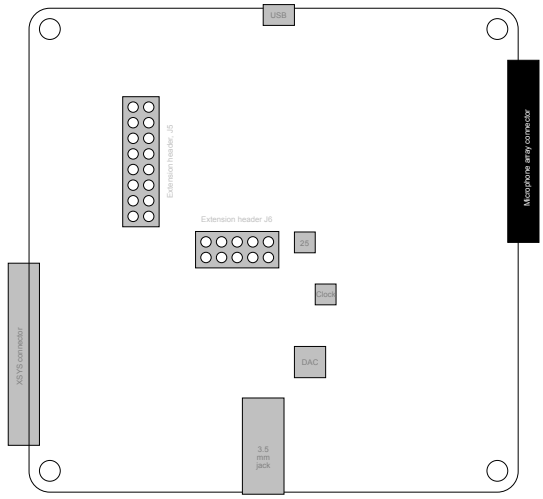

Figure 6: Microphone connector location

The microphone array consists of a linear array of four microphones (spaced 33mm apart), a clock buffer, voltage level shifters and an EEPROM for optional identification.

The microphone signals are mapped onto the XVF3000 device as shown in Figure 7.

Figure 7: Linear MEMS microphone board xCORE GPIO

Microphone	xCORE GPIO	Port
MIC_CLK	X0D12	P1E0
MCLK_IN	X0D13	P1F0
MIC_0	X0D14	P8B0
MIC_1	X0D15	P8B1
MIC_2	X0D16	P8B2
MIC_3	X0D17	P8B3

6 I2C bus

The BaseBoard has a main I2C bus that is used to control the DAC, clock generator, and EEPROM. This main I2C bus is connected to tile 1 of the XVF3000, with the XVF3000 acting as a master on this I2C bus.

Pin	Port	Signal
X1D26	P4E0	I2C_SCL
X1D27	P4E1	I2C_SDA

The addresses of devices on the I2C bus are shown below.

Device	Address	
Si5351A (Clock)	0b1100010	0x62
CS43L21 (DAC)	0b1001010	0x4A
24LC08B (EEPROM on microphone board)	0b1010Xxx	0x5x

Please refer to the 24LC08B datasheet for details on how to set the address of the EEPROM.

The BaseBoard also has a secondary I2C bus, on which the XVF3000 is a slave - so allowing the XVF3000 to be controlled by an external I2C host. This slave I2C interface is wired up to the extension header (see §8, below).

7 General purpose user interface

The BaseBoard has 13 LEDs that are controlled by the XVF3000 GPIO. LED_0 - LED_11 (D2-D13) are positioned around the edge of the BaseBoard. LED_12 (D14) is positioned in the middle of the BaseBoard. The LED GPIO output must be set low to light the corresponding LED.

Four general purpose push-button switches are provided. When pressed, each button creates a connection from the I/O to GND. To ensure correct behavior, the port connected to the buttons (P4A) must always be defined as an input.

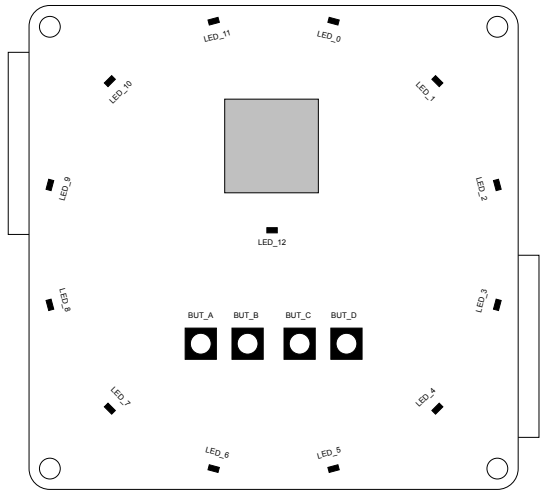

Figure 8: General purpose user interface components

The signal mapping of the user interface components is shown in Figure 9 and Figure 10

UI signal	xCORE GPIO	Port
BUTTON_A	X0D02	P4A0
BUTTON_B	X0D03	P4A1
BUTTON_C	X0D08	P4A2
BUTTON_D	X0D09	P4A3

Figure 9: User interface GPIO

A green LED (PGOOD) near the USB connector indicates 3V3 and 1V0 supplies are up.

UI signal	xCORE GPIO	Port
LED_0	X0D26	P16B0
LED_1	X0D27	P16B1
LED_2	X0D28	P16B2
LED_3	X0D29	P16B3
LED_4	X0D30	P16B4
LED_5	X0D31	P16B5
LED_6	X0D32	P16B6
LED_7	X0D33	P16B7
LED_8	X0D34	P1K0
LED_9	X0D35	P1L0
LED_10	X0D36	P16B8
LED_11	X0D37	P16B9
LED_12	X0D38	P16B10

Figure 10: User interface GPIO

8 Extension headers

The BaseBoard has a two extension headers, J5 and J6, containing: audio MCLK, all I2S signals, the secondary I2C bus (see §6) and seven general purpose IOs controlled by the XVF3000.

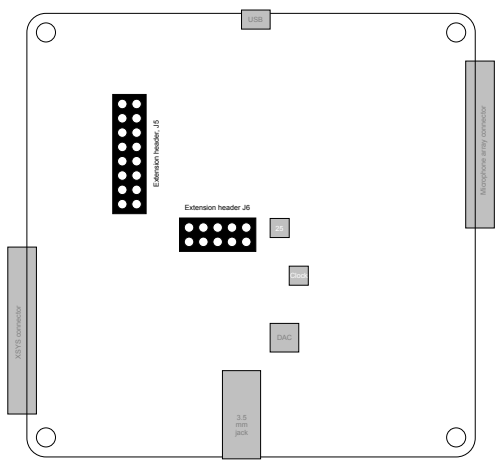

Figure 11: Extension header location

The signal mapping of the extension header is shown in Figure 12 and Figure 13.

These signals allow the XVF3000 to be connected to an external applications processor host. In the following descriptions:

- *input* means captured voice audio that is sent from the XVF3000 to the host.
- *output* means audio sent from the host to the XVF3000, to be played out from the DAC.

The software pre-flashed in to the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** configures the XVF3000 device and BaseBoard hardware to use these extension headers; to enable I2S audio input/output connectivity (XVF3000 is the I2S master) and I2C control (XVF3000 is an I2C slave).

- XVF3000 as I2S master

  Audio input and output connectivity is provided via I2S, via pins 1, 3, 6 of J6 and pin 4 of J5.

  I2S_DAC_DATA is the audio output from the host for the DAC far-end signal.

  I2S_ADC_DATA is the audio input to the host from the XVF3000.

  MasterClock is generated by the XVF3000 and provided on pin 7 of J6 for connection to the host.

- XVF3000 as I2C slave

  I2C control is provided via pins 9 and 12 on J5.

  This is the secondary XVF3000 I2C bus, on which the XVF3000 is a slave (see §6).

  Pull-up resistors should be put on I2C_SDA_EXT and I2C_SCL_EXT.

The XVF3000 device and BaseBoard hardware *can* support other modes of audio connectivity and control. These modes are documented here for reference only - their use requires a different XVF3000 software.

- XVF3000 as I2S slave.

  Audio input and output connectivity is provided via I2S, via pins 1, 3, 6 of J6 and pin 4 of J5.

  I2S_DAC_DATA is the audio output from the host for the DAC far-end signal.

  I2S_ADC_DATA is the audio input to the host from the XVF3000.

  A 24.576 MHz MasterClock should be generated externally and connected to the BaseBoard via pin 15 of J5. To use this mode, remove R67 and insert a 0R link into R17.

- XVF3000 as USB audio and control device.

  Input audio from the XVF3000 and output audio to the DAC is communicated over USB, and the XVF3000 device is controlled over USB.

  In this mode, extension headers should be left unconnected.

Header pin J5	xCORE GPIO	Port	Signal
1	X0D22	P1G0	
2			GND
3	X0D23	P1H0	
4	X1D35	P1L0	I2S_ADC_DATA
5	X0D00	P1A0	
6			GND
7	X0D11	P1D0	
8			GND
9	X0D24	P1I0	I2C_SDA_EXT
10	X0D39	P1P0	
11			GND
12	X0D25	P1J0	I2C_SCL_EXT
13			3V3
14			GND
15			EXT_MCLK
16			GND

Figure 12: Extension header GPIO J5

Header pin J6	xCORE GPIO	Port	Signal
1	X1D37	P1N0	I2S_LRCK
2	GND		
3	X1D39	P1P0	I2S_DAC_DATA
4	NC		
5	GND		
6	X1D36	P1M0	I2S_BCLK
7	X1D38	P1O0	MCLK_TILE1
8	GND		
9	X1D11	P1D0	
10	X1D10	P1C0	

Figure 13: Extension header GPIO J6

9 USB port

The USB micro-B port (J1) provides power for all the on-board circuits and is used to generate the following voltage rails:

- +1V0 (Core voltage to XMOS device)
- +2V5 (for headphone amplifier in DAC device)
- +3V3 for GPIOs and other accessory devices

Voltage tolerance should be as per USB VBUS specification values.

Proper power-on sequence is indicated by power good LED (D1) in bottom side of the board.

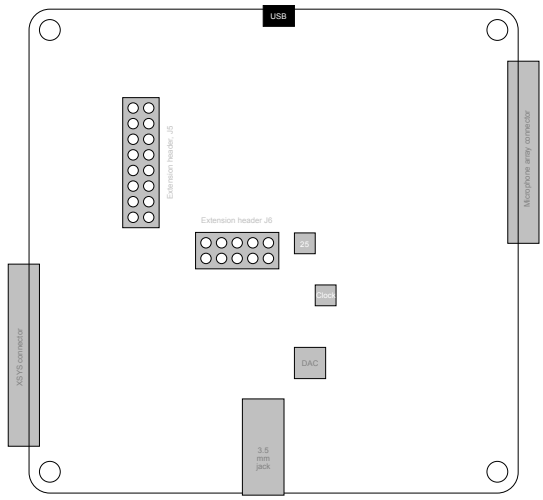

Figure 14: USB components

The data lines from the USB micro-B port (J1) are connected to the XVF3000's integrated USB PHY, and so (with a different XVF3000 software) *can* be used to provide USB audio and/or control connectivity to the XVF3000 and the BaseBoard.

Note:

- the software pre-flashed in to the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** does **not** provide any USB connectivity.
- J1 must be connected at all times to provide power to the BaseBoard, even though the USB interface is not used.

10 Flash memory

The XVF3000 device includes 2MBytes of QSPI flash memory, which is interfaced by the GPIO connections shown in Figure 15:

QSPI connection	Pin	Port
QSPI_SS	X0D01	P1B
QSP_D0	X0D04	P4B0
QSP_D1	X0D05	P4B1
QSP_D2	X0D06	P4B2
QSP_D3	X0D07	P4B3
SPI_CLK	X0D10	P1C

Figure 15: QSPI Flash

11 xSYS connector

A standard XMOS xSYS interface (J2) is provided to allow host debug of the board via JTAG.

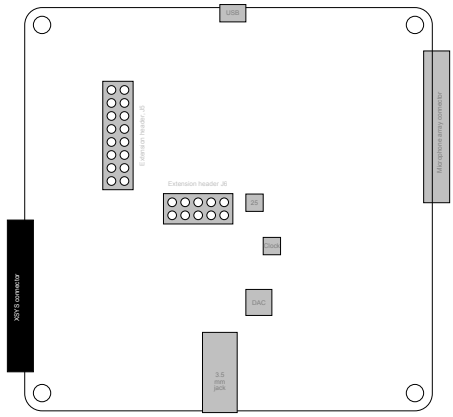

Figure 16: XSYS connector

xSYS signal	xCORE GPIO	Header pin	Description
TMS	See note	7	JTAG Test Mode Select
TCK	See note	9	JTAG Test Clock
TDI	See note	5	JTAG Test Data In - from debug adapter to xCORE
TDO	See note	13	JTAG Test Data Out - from xCORE to debug adapter
RST_N	See note	15	System Reset - active low, resets xCORE device
GND		4, 8, 12, 16, 20	Ground
XL_UP1	X0D43	6	XMOS link, uplink bit 1
XL_UP0	X0D42	10	XMOS link, uplink bit 0
XL_DN0	X0D40	14	XMOS link, downlink bit 0
XL_DN1	X0D41	18	XMOS link, downlink bit 1

Figure 17: xSYS Connector Pinout

Notes:

- JTAG connections occupy dedicated connections

12 xCORE VocalFusion BaseBoard portmap

The table below provides a full description of the port-pin mappings described throughout this document for the xCORE VocalFusion BaseBoard.

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X0D00	$1A^0$					
X0D01	$1B^0$					QSPI_CS
X0D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	BUTTON_A
X0D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	BUTTON_B
X0D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	QSPI_D0
X0D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	QSPI_D1
X0D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	QSPI_D2
X0D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	QSPI_D3
X0D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	BUTTON_C
X0D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	BUTTON_D
X0D10	$1C^0$					QSPI_CLK
X0D11	$1D^0$					
X0D12	$1E^0$					MIC_CLK
X0D13	$1F^0$					MCLK_IN
X0D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	MIC_0
X0D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	MIC_1
X0D16		$4D^0$	$8B^2$	$16A^{10}$		MIC_2
X0D17		$4D^1$	$8B^3$	$16A^{11}$		MIC_3
X0D18		$4D^2$	$8B^4$	$16A^{12}$		MIC_4
X0D19		$4D^3$	$8B^5$	$16A^{13}$		MIC_5
X0D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	MIC_6
X0D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	MIC_7
X0D22	$1G^0$					
X0D23	$1H^0$					
X0D24	$1I^0$					
X0D25	$1J^0$					
X0D26		$4E^0$	$8C^0$	$16B^0$		LED_0
X0D27		$4E^1$	$8C^1$	$16B^1$		LED_1
X0D28		$4F^0$	$8C^2$	$16B^2$		LED_2
X0D29		$4F^1$	$8C^3$	$16B^3$		LED_3
X0D30		$4F^2$	$8C^4$	$16B^4$		LED_4
X0D31		$4F^3$	$8C^5$	$16B^5$		LED_5
X0D32		$4E^2$	$8C^6$	$16B^6$		LED_6
X0D33		$4E^3$	$8C^7$	$16B^7$		LED_7
X0D34	$1K^0$					LED_8
X0D35	$1L^0$					LED_9
X0D36	$1M^0$		$8D^0$	$16B^8$		LED_10
X0D37	$1N^0$		$8D^1$	$16B^9$		LED_11
X0D38	$1O^0$		$8D^2$	$16B^{10}$		LED_12
X0D39	$1P^0$		$8D^3$	$16B^{11}$		
X0D40			$8D^4$	$16B^{12}$		XL_DN1
X0D41			$8D^5$	$16B^{13}$		XL_DN0
X0D42			$8D^6$	$16B^{14}$		XL_UP0
X0D43			$8D^7$	$16B^{15}$		XL_UP1

Figure 18: xCORE VocalFusion Base Board-Portmap: Tile 0

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X1D00	$1A^0$					
X1D01	$1B^0$					
X1D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	
X1D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	
X1D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	
X1D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	
X1D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	
X1D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	
X1D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	
X1D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	
X1D10	$1C^0$					
X1D11	$1D^0$					
X1D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	
X1D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	
X1D16		$4D^0$	$8B^2$	$16A^{10}$		
X1D17		$4D^1$	$8B^3$	$16A^{11}$		
X1D18		$4D^2$	$8B^4$	$16A^{12}$		
X1D19		$4D^3$	$8B^5$	$16A^{13}$		
X1D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	
X1D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	
X1D26		$4E^0$	$8C^0$	$16B^0$		I2C_SCL
X1D27		$4E^1$	$8C^1$	$16B^1$		I2C_SDA
X1D28		$4F^0$	$8C^2$	$16B^2$		DAC_RST_N
X1D29		$4F^1$	$8C^3$	$16B^3$		
X1D30		$4F^2$	$8C^4$	$16B^4$		
X1D31		$4F^3$	$8C^5$	$16B^5$		
X1D32		$4E^2$	$8C^6$	$16B^6$		
X1D33		$4E^3$	$8C^7$	$16B^7$		
X1D35	$1L^0$					
X1D36	$1M^0$		$8D^0$	$16B^8$		I2S_BCLK
X1D37	$1N^0$		$8D^1$	$16B^9$		I2S_LRCK
X1D38	$1O^0$		$8D^2$	$16B^{10}$		MCLK_TILE1
X1D39	$1P^0$		$8D^3$	$16B^{11}$		I2S_DAC_DATA
X1D40			$8D^4$	$16B^{12}$		
X1D41			$8D^5$	$16B^{13}$		
X1D42			$8D^6$	$16B^{14}$		
X1D43			$8D^7$	$16B^{15}$		

Figure 19: xCORE VocalFusion BaseBoard Portmap: Tile 1

13 Operating requirements

A USB 2.0 high-speed compliant cable of less than 3m in length should be used when operating the **xCORE VocalFusion 4-Mic Kit for Amazon AVS**. XMOS cannot guarantee correct operation of the base board should any other cable be used.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the **xCORE VocalFusion 4-Mic Kit for Amazon AVS** with appropriate ESD precautions in place.

14 Dimensions

The BaseBoard is 90x90mm square with a board thickness of 1.6mm.

15 RoHS and REACH

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The **xCORE VocalFusion 4-Mic Kit for Amazon AVS** is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.

16 Schematics

The schematics for the Base Board included in the kit, are shown in the first five figures below, followed by the schematics for the linear array board.

For full reference schematics please contact XMOS:

- https://www.xmos.com/contact/enquiries

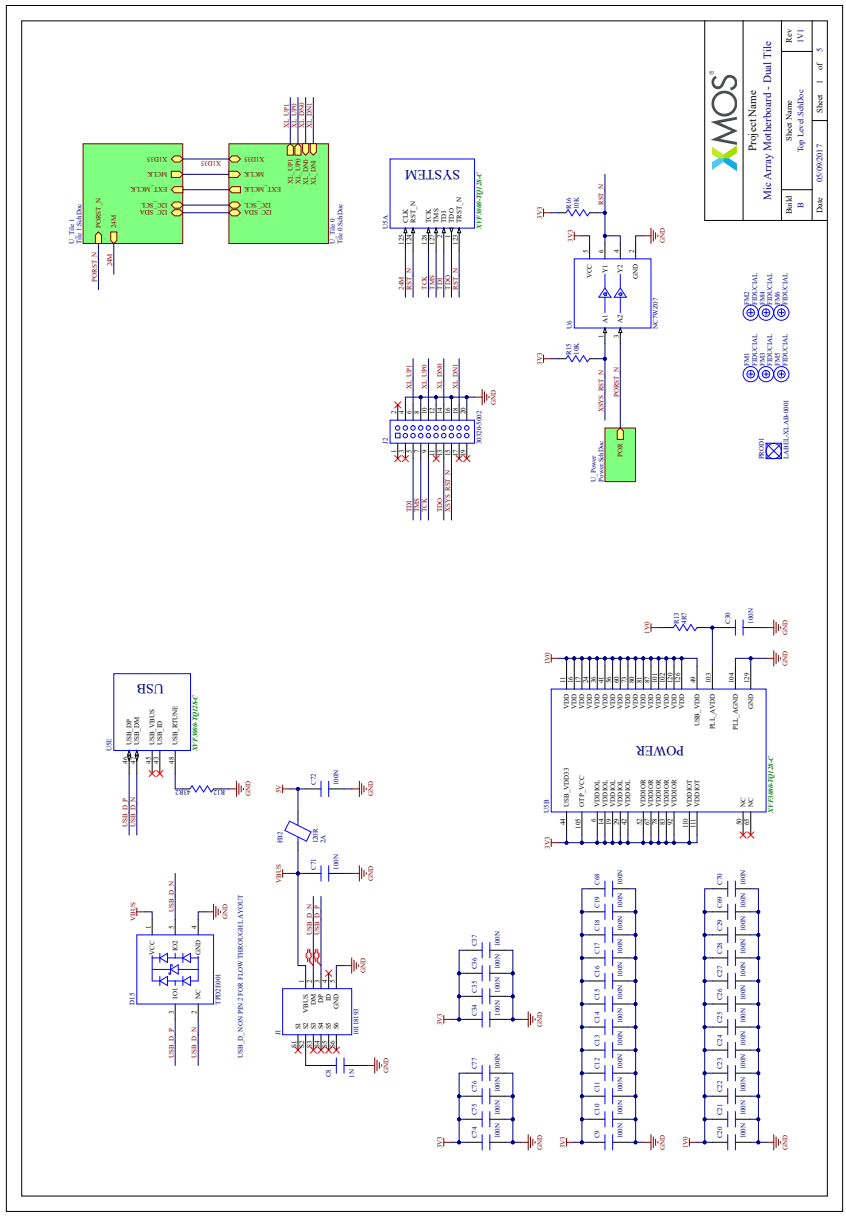

Figure 20: xCORE VocalFusion BaseBoard - XVF3000 configuration

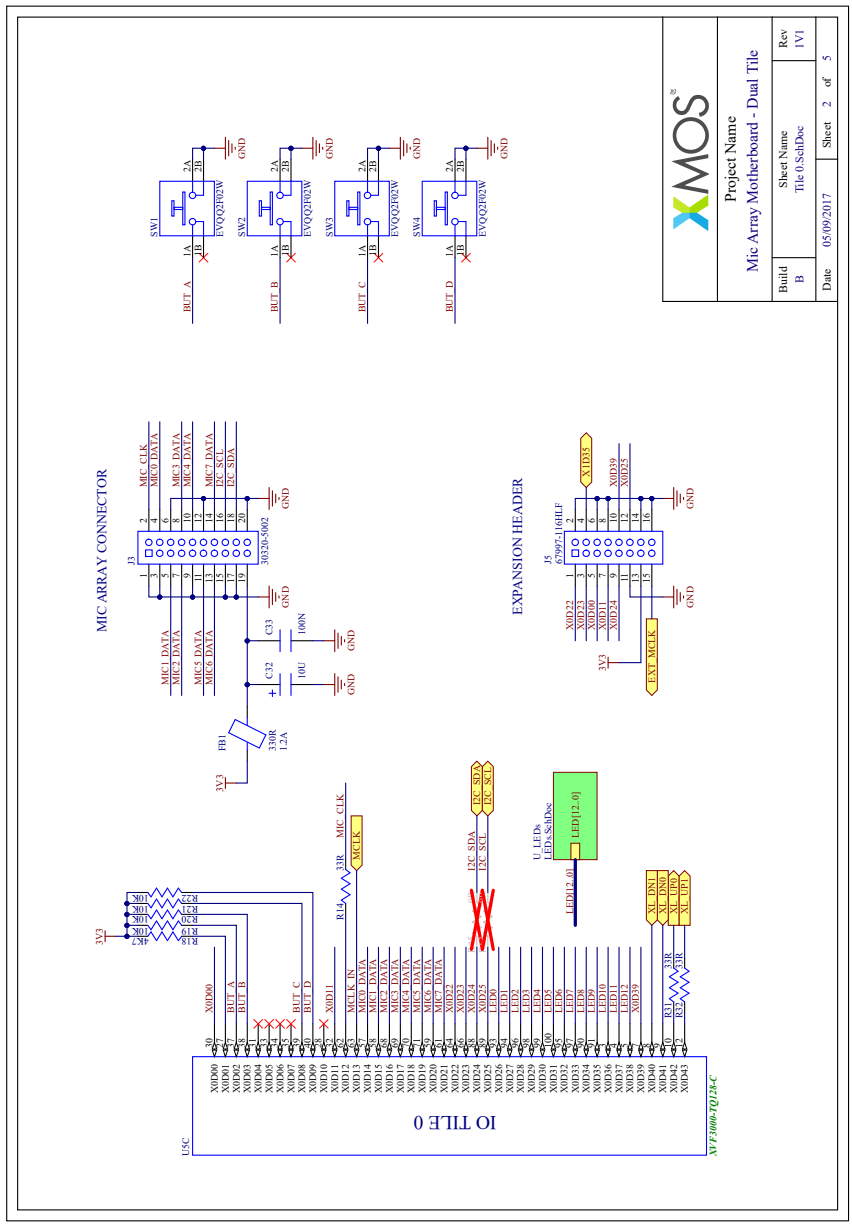

Figure 21: xCORE VocalFusion BaseBoard - extension header, buttons, Microphone header, Tile 0 IO

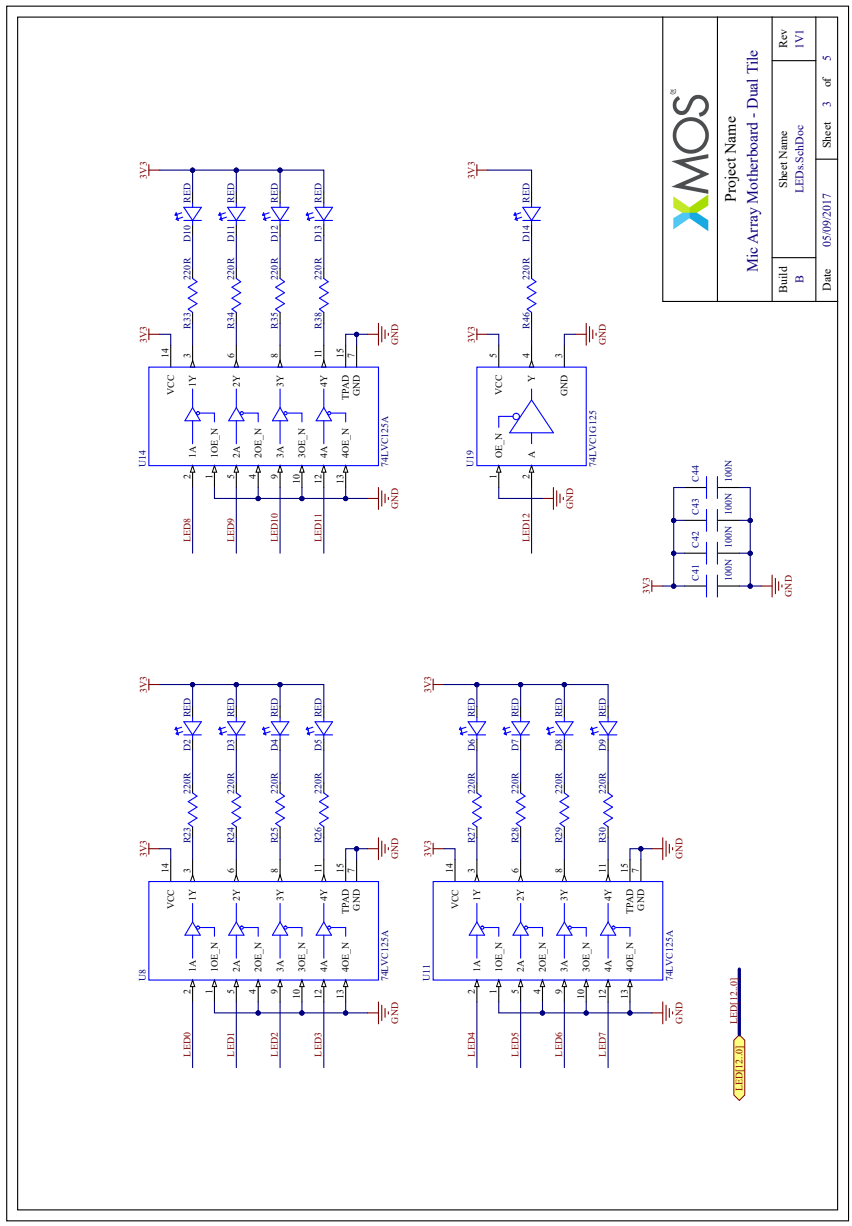

Figure 22: xCORE VocalFusion BaseBoard - LEDs

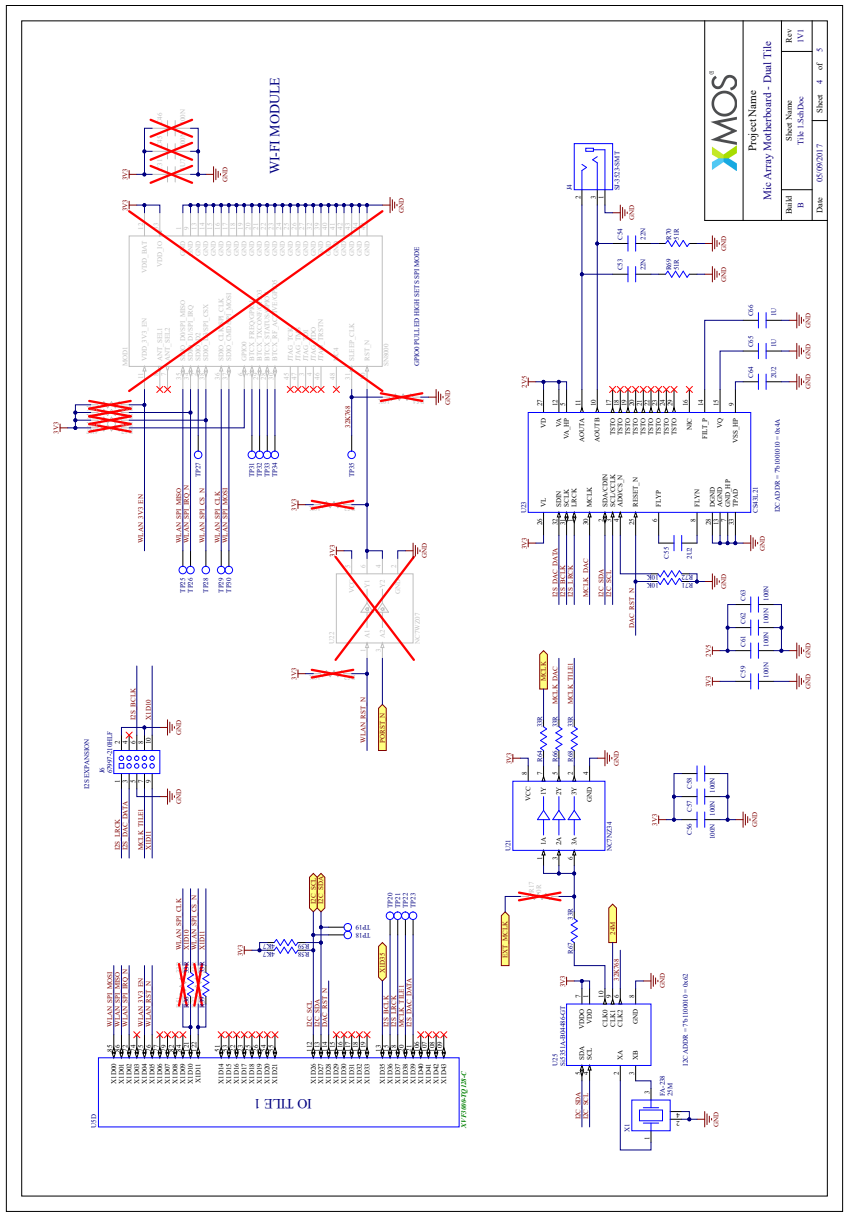

Figure 23: xCORE VocalFusion BaseBoard - Clock and stereo DAC with headphone jack circuitry, tile 1 IO

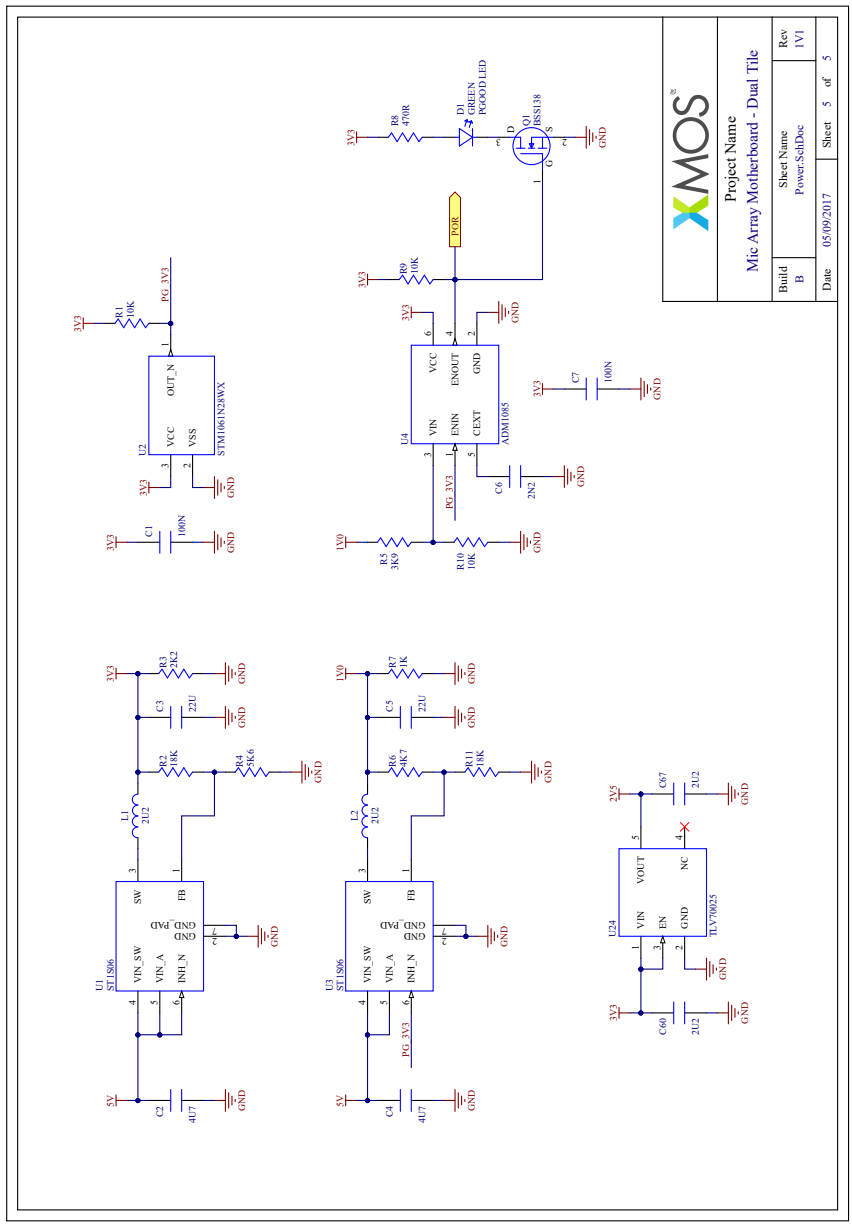

Figure 24: xCORE VocalFusion BaseBoard - voltage rail LDOs and reset circuit

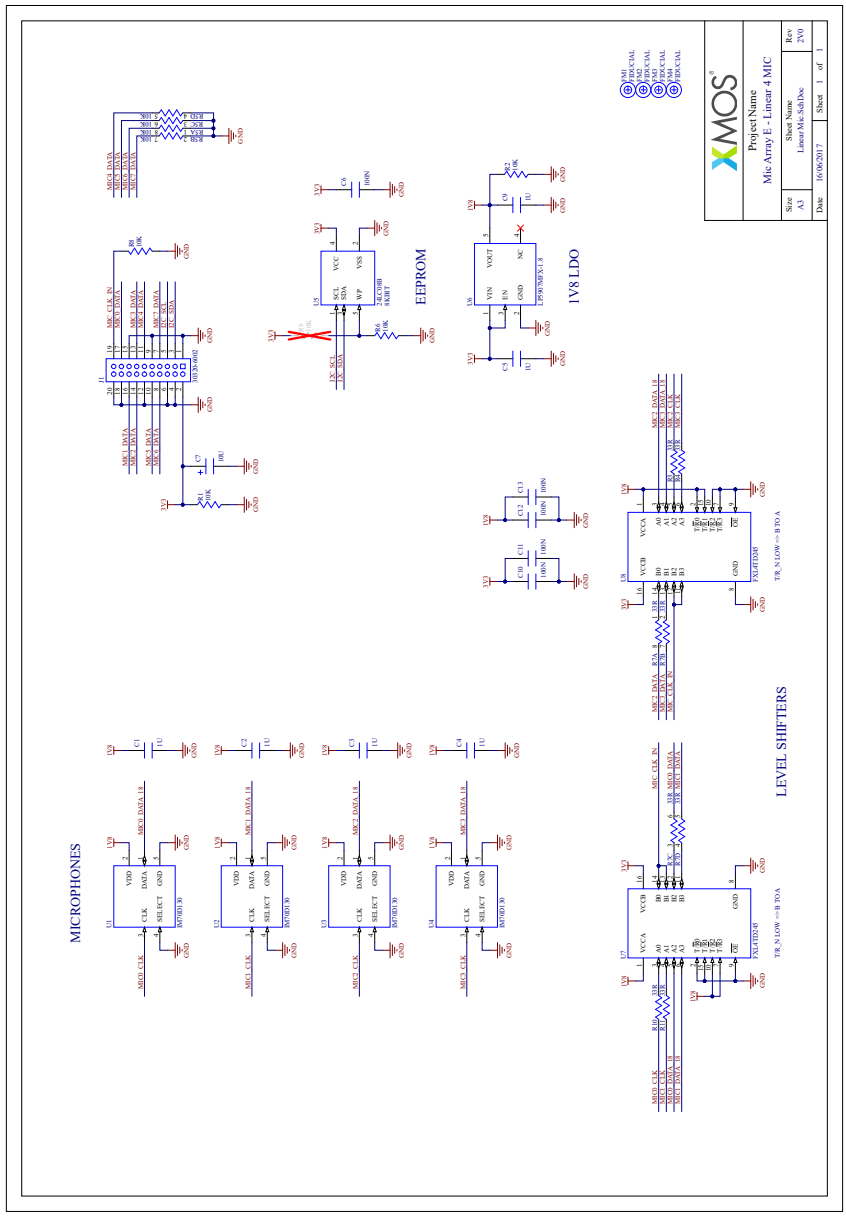

Figure 25: xCORE VocalFusion - Linear Microphone Board