

xCORE-200 XU/XUF USB

A new generation of high performance USB-enabled multicore microcontrollers



FEATURES

Multicore compute with up to 1000MIPS (8 core) and 4000MIPS (32 core) performance.

Hardware Response[™] ports provide flexible, high-performance configurable I/O capability.

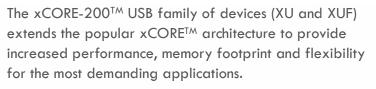
Integrated USB 2.0 PHY for highand full-speed host and device operation.

Up to 1024KB on-board memory for demanding applications.

Embedded flash option – up to 2048KB on-board.

Free software library support to implement your exact mix of peripherals.

Easy to use with our free xTIMEcomposer Studio[™] tools.



xCORE-200 XU/XUF integrates up to two USB 2.0 PHYs (host or device) and implements a dual-issue processor pipeline to boost peak compute performance up to 4000MIPS and 2000MMACS.

Up to 1024KB on-chip SRAM memory is available. Each member of the xCORE-200 family has an embedded flash option for applications.

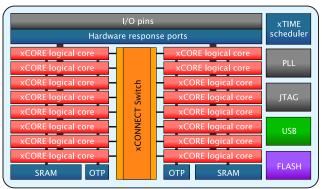
The flexible Hardware Response ports are bonded out to I/O pins as 1 bit, 4 bit, 8 bit, 16 bit and 32 bit ports, and provide support for serialized and buffered data transfer. Up to 256 general purpose I/O are available for user configuration.

xCORE-200 is supported by the advanced XMOS xTIMEcomposer StudioTM development environment, and a wide range of microcontroller and application libraries are freely downloadable from <u>www.xmos.com</u>



xCORE-200 USB PRODUCT BRIEF

Unlike conventional microcontrollers, xCORE-200 multicore microcontrollers execute multiple realtime tasks simultaneously. The xCORE-200 XU/XUF family includes devices with 8, 10, 12, 16, 24 and 32 cores. Each logical core can execute computational code, advanced DSP code, control software (including logic decisions and executing a state machine) or drive and sample data on the I/O ports.



The devices include xTIME scheduling hardware

xCORE-200[™] XUF216

that performs functions similar to those of an RTOS, and hardware that connects the cores directly to I/O pins, ensuring fast processing and extremely low latency. The xTIME scheduler eliminates the use of interrupts and ensures deterministic operation.

The on-chip SRAM can be accessed in a single cycle, reducing shared memory requirements by passing data directly between tasks executing on logical cores. Similarly the xCONNECT switch is a high-speed network allowing all cores to communicate with each other.

xCORE-200 multicore microcontrollers include an area of one-time programmable memory with AES support to allow the implementation of secure boot functionality.

ORDERING INFORMATION

xCORE-200 XU/XUF devices are available in a range of resource densities, packages, performance and temperature grades depending on your needs.

	-				Package [GPIOs]			
Family	Cores	RAM (KB)	Flash (KB)	USB PHYs	TQ64	TQ128	FB236	FB374
XU208	8	128 256	-	1	XU208-128-TQ64 [33] XU208-256-TQ64 [33]	XU208-128-TQ128 [33] XU208-256-TQ128 [33]		
XU210	10	256 512	-	1		XU210-256-TQ128 [81] XU210-512-TQ128 [81]	XU210-256-FB236 [128] XU210-512-FB236 [128]	
XU212	12	256 512	-	1		XU212-256-TQ128 [81] XU212-512-TQ128 [81]	XU212-256-FB236 [128] XU212-512-FB236 [128]	
XU216	16	256 512	-	1		XU216-256-TQ128 [81] XU216-512-TQ128 [81]	XU216-256-FB236 [128] XU216-512-FB236 [128]	
XU224	24	512 1024	-	2				XU224-512-FB374 [256] XU224-1024-FB374 [256]
XU232	32	512 1024	-	2				XU232-512-FB374 [256] XU232-1024-FB374 [256]
XUF208	8	128 256	1024	1	XUF208-128-TQ64 [33] XUF208-256-TQ64 [33]	XUF208-128-TQ128 [33] XUF208-256-TQ128 [33]		
XUF210	10	256 512	2048	1			XUF210-256-FB236 [128] XUF210-512-FB236 [128]	
XUF212	12	256 512	2048	1			XUF212-256-FB236 [128] XUF212-512-FB236 [128]	
XUF216	16	256 512	2048	1			XUF216-256-FB236 [128] XUF216-512-FB236 [128]	
XUF224	24	512 1024	2048	2				XUF224-512-FB374 [256] XUF224-1024-FB374 [256]
XUF232	32	512 1024	2048	2				XUF232-512-FB374 [256] XUF232-1024-FB374 [256]

For pricing and availability, please visit the XMOS website for a list of our distributors. www.xmos.com/distributors.



© 2015 XMOS LTD

Third party trademarks are hereby acknowledged. This is a preliminary product brief, contents are subject to change.

XM-006870-PC | 2015-08-12