xCORE-200 Multichannel Audio Platform 2v0 Hardware Manual

IN THIS DOCUMENT

The xCORE-200 Multichannel Audio Platform (XK-AUDIO-216-MC-AB) is a complete hardware and reference software platform targeted at up to 32-channel USB and networked audio applications, such as DJ decks and mixers.

The Multichannel Audio Platform hardware is based around the XE216-512-TQ128 multicore microcontroller; an xCORE-200 device with an integrated High Speed USB 2.0 PHY, RGMII (Gigabit Ethernet) interface and 16 logical cores delivering up to 2000MIPS of deterministic and responsive processing power.

Exploiting the flexible programmability of the xCORE-200 architecture, the Multichannel Audio Platform supports either USB or network audio source, streaming 8 input and 8 output audio channels simultaneously - at up to 192kHz. Ideal for mixing two sources and providing main and headphone monitor output feeds.

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XMOS

The guaranteed Hardware-Response™ times of xCORE technology always ensure lowest latency (round trip as low as 3ms), bit perfect audio streaming to and from the USB host or network.

Delivered as source code, the reference software provides a fully featured production ready solution, including support for:

- Full-Speed and High-Speed USB operation, Audio Class 2.0 & 1.0, MIDI, HID and DFU classes.
- Standards compliant AVB Talker and/or Listener endpoints
- MFi support for Apple Host Mode and USB Role Switch

1 Features

A block diagram of the xCORE-200 Multichannel Audio Platform (XK-AUDIO-216-MC-AB) is shown below:

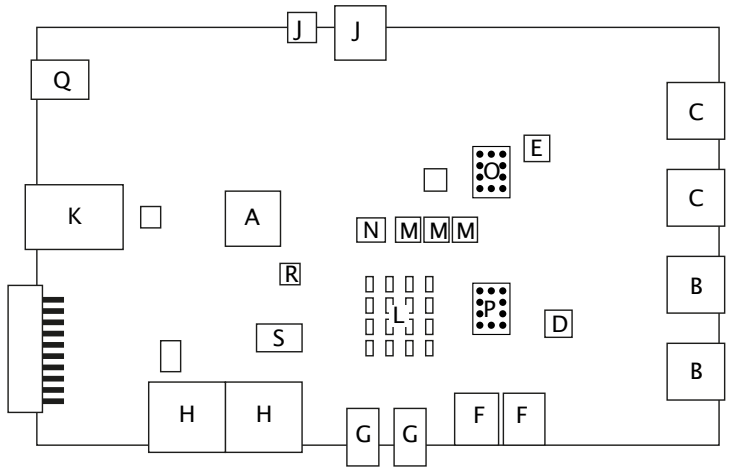

Figure 1: xCORE-200 Multichannel Audio Platform block diagram

It includes the following features:

- A: xCORE-200 (XE216-512-TQ128) Multicore Microcontroller device
- B: 8 output analog audio channels (3.5mm stereo jack)
- C: 8 input analog audio channels (3.5mm stereo jack)
- D: 192kHz 24b audio DAC
- E: 192kHz 24b audio ADC
- F: Optical connections for digital interface (e.g. S/PDIF and ADAT)

- G: Coaxial connections for digital interfaces (e.g. S/PDIF)
- H: MIDI in and out connections
- I: An ultra low-jitter programmable audio phase lock loop
- J: USB 2.0 type A and micro-B jacks
- K: 10/100/1000 Mbps Ethernet connection
- L: 16 general purpose LEDs
- M: 3 general purpose buttons
- N: 1 general purpose 2-way switch
- O: Selectable TDM input audio sources
- P: Selectable TDM output audio sources
- Q: Integrated power supply unit
- R: Quad-SPI boot ROM
- S: 24MHz Oscillator

2 xCORE Multicore Microcontroller Device

xCORE-200 Multichannel Audio Platform (XK-AUDIO-216-MC-AB) is based on a two-tile xCORE-200 device (XE216-512-TQ128). Each tile is user-programmable, providing eight logical cores with a total of up to 1000 MIPS compute. A total of 53 general-purpose digital I/O have been brought out to header pins, providing tremendous flexibility for a wide range of USB and networked audio products to be developed on a common platform.

For information on xCORE-200 tiles and cores see the xCORE-200 Architecture Overview[1].

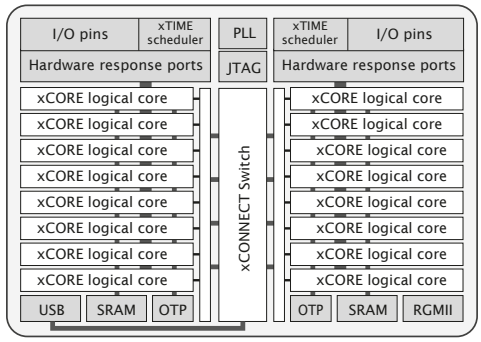

Figure 2: xCORE-200 device

3 Analog input audio channels

A total of eight single-ended analog input channels are provided via 3.5mm stereo jacks. Each is fed into a CirrusLogic CS5368 ADC.

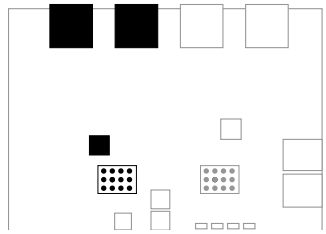

Figure 3: Analog input stage

The four digital input channels SDIN1 to SDIN4 are mapped to the xCORE inputs xSDIN1 to xSDIN4 through a header array as described in Figure 4. The jumper allows channel selection when the DAC is used in TDM mode

Row 1, column 1 is defined as the pin closest to pin 1 of the header (as denoted by a triangle on the silk-screen).

The ADC registers are accessed via the I2C bus - see §12.

[1] http://www.xmos.com/published/xcore-architecture

Row	Column 1	Column 2	Column 3
1	ADC_SD1	iADC_SD1	ADC_SD1
2	ADC_SD2	iADC_SD2	ADC_SD1
3	ADC_SD3	iADC_SD3	ADC_SD1
4	ADC_SD4	iADC_SD4	ADC_SD1

Figure 4: Analog input patching

The xSDIN signals are connected to both 1b and 4b ports of the xCORE-200 IO as described in Figure 5. This allows additional flexibility in the firmware.

Audio output	xCORE GPIO	Port	Description
iADC_SD1	X0D24	P1I	Analog input 1 (DSD_MODE = 0)
iADC_SD2	X0D25	P1J	Analog input 2 (DSD_MODE = 0)
iADC_SD3	X0D34	P1K	Analog input 3 (DSD_MODE = 0)
iADC_SD4	X0D35	P1L	Analog input 4 (DSD_MODE = 0)
OVERFLOW	X0D15	P4C1	Active low overflow
ADC_RST_N	X0D32	P4E2	Active low reset
LRCLK	X0D22	P1G	Serial audio channel clock
SCLK	X0D23	P1H	Main timing for serial audio interface
MCLK_AUDIO	See notes below		ADC master clock

Figure 5: Analog input xCORE GPIO

Notes:

- Details of the analog input stage clocking scheme can be found in §8.

4 Analog output audio channels

A total of eight single-ended analog output channels are provided. Each is fed into a CirrusLogic CS4384 DAC.

The four digital output channels SDOUT1 to SDOUT4 are mapped to the xCORE inputs xSDOUT1 to xSDOUT4 through a header array as described in Figure 7.

Row 1, column 1 is defined as the pin closest to pin 1 of the header (as denoted by a triangle on the silk-screen).

The ADC registers are accessed via the I2C bus - see §12.

The xSDOUT signals are connected to the xCORE-200 IO as described in Figure 8

Notes:

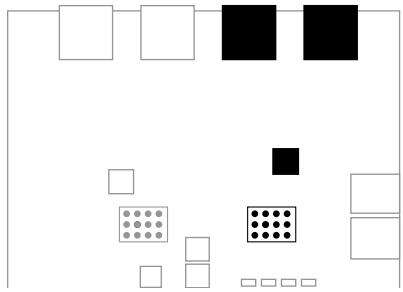

Figure 6: Analog output stage

Row	Column 1	Column 2	Column 3
1	DAC_SD1	xDAC_SD1	DAC_SD1
2	DAC_SD2	xDAC_SD2	DAC_SD1
3	DAC_SD3	xDAC_SD3	DAC_SD1
4	DAC_SD4	xDAC_SD4	DAC_SD1

Figure 7: Analog output patching

Audio output	xCORE GPIO	Port	Description
DAC_SD5	X0D24	P1I	DAC DSD5 (DSD_MODE = 1)
DAC_SD6	X0D25	P1J	DAC DSD6 (DSD_MODE = 1)
DAC_SD7	X0D34	P1K	DAC DSD7 (DSD_MODE = 1)
DAC_SD8	X0D35	P1L	DAC DSD8 (DSD_MODE = 1)
xDAC_SD1	X0D36 | P1M		DAC SD/DSD1
xDAC_SD2	X0D37 | P1N		DAC SD/DSD2
xDAC_SD3	X0D38 | P1O		DAC SD/DSD3
xDAC_SD4	X0D39 | P1P		DAC SD/DSD4
DAC_RST_N	X0D27	P4E1	Active low reset
LRCLK	X0D22	P1G	Serial audio channel clock
SCLK	X0D23	P1H	Main timing for serial audio interface
MCLK_AUDIO	See notes below		DAC master clock

Figure 8: Analog output xCORE GPIO

- Details of the analog input stage clocking scheme can be found in §8.

5 Digital audio output

Optical and coaxial digital audio transmitters are used to provide digital audio output in formats such as IEC60958 consumer mode (S/PDIF) and ADAT.

The data streams from the xCORE-200 are re-clocked using the external master clock to synchronise the data into the audio clock domain. This is achieved using simple external D-type flip-flops.

The optical output uses a TOSLINK optical connector with an integrated LED and differential driving circuit. The coaxial output uses an RCA connector and is isolated via a transformer.

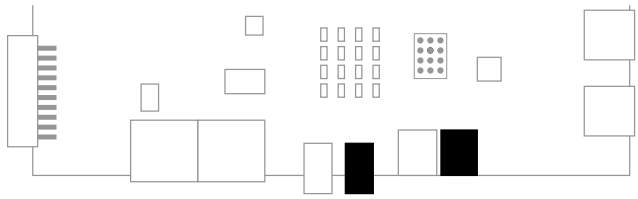

Figure 9: Optical audio output

The signals are generated from two 1-bit ports on the xCORE-200.

Audio signal	xCORE GPIO	Port	Description
OPT_TX	X0D12	P1E	For use with either S/PDIF or ADAT
COAX_TX	X0D11	P1D	For use with either S/PDIF or ADAT
MCLK_DIG	See notes below		Digital master clock

Figure 10: Optical output audio xCORE GPIO

Notes:

- Details of the analog input stage clocking scheme can be found in §8.

6 Digital audio input

Digital audio input is provided to allow formats such as IEC60958 consumer mode (S/P DIF) or ADAT to be connected to the device via either optical or coaxial mediums.

The optical input uses a TOSLINK optical connector with an integrated photodiode and receiver circuit. The coaxial input uses an RCA connector and is AC-coupled into a 75Ω terminator.

This gives a signal level of $0.5V_{p\text{-}p}$, which is fed into a differential line receiver.

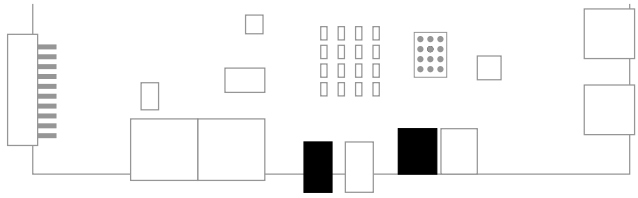

Figure 11: Optical audio input

The input signals are fed into two 1-bit ports on the xCORE-200 device.

Audio signal	xCORE GPIO	Port	Description
OPT_RX	X1D38	P1O	For use with either S/PDIF or ADAT
COAX_RX	X1D39	P1P	For use with either S/PDIF or ADAT
MCLK_DIG	See notes below		Digital master clock

Figure 12: Optical audio input xCORE GPIO

Notes:

- Details of the analog input stage clocking scheme can be found in §8.

7 MIDI audio input and output

MIDI I/O is provided on the board via a standard Gameport connector. The signals are buffered using 5V line drivers and are then connected to 1-bit ports on the xCORE-200, via a 5V to 3.3V buffer.

10Ω pull ups are placed on the MIDI IN signal from the connector and on the MIDI OUT signal from the xCORE-200. These stop glitches on startup and when no MIDI devices are connected to the board

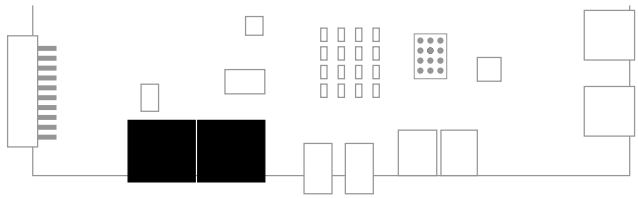

Figure 13: MIDI audio input/output

The MIDI audio signals are connected to the xCORE-200 IO, as described in Figure 14, via a 5V to 3.3V buffer.

Audio signal	xCORE GPIO	Port	Description
MIDI_TX	X1D37	P1N	
MIDI_RX	X1D36	P1M	

Figure 14: MIDI audio xCORE GPIO

8 Audio clocking

A flexible clocking scheme is provided for both audio and other system services.

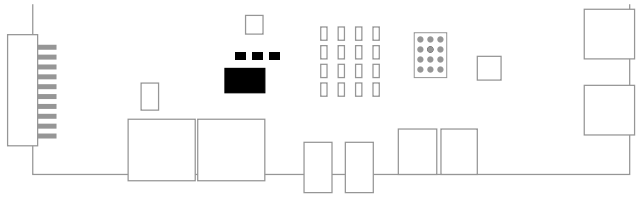

Figure 15: Clocking circuit

In order to accommodate a multitude of clocking options, the low-jitter master clock is generated locally using a frequency multiplier PLL chip. The chip used is a Phaselink PL611-01, which is pre-programmed to provide a 24MHz clock from its CLK0 output, and either 24.576 MHz (FSEL high) or 22.5792MHz (FSEL low) from its CLK1 output.

The 24MHz fixed output is provided to the xCORE-200 device, as the main processor clock. It also provides the reference clock to a CirrusLogic CS2100, which provides a very low jitter audio clock from a synchronisation signal provided from the xCORE-200.

Either the locally generated clock (from the PL611) or the recovered low jitter clock (from the CS2100) may be selected to clock the audio stages; the xCORE-200, the ADC/DAC and Digital output stages.

Audio signal	xCORE GPIO	Port	Description
MCLK_FSEL	X0D33	P4E3	Set local clock to 24.576 MHz (MCLK_FSEL high) or 22.5792MHz (MCLK_FSEL low)
PLL_SYNC	X0D0	P1A	Reference clock from xCORE-200
PLL_SELECT	X0D31	P4F3	Select local fixed clock (SELECT low) or PLL output (SELECT high)
MCLK_XCORE	X0D13, X1D35	P1F, P1L	Audio clock to xCORE audio path

The CirrusLogic CS2100 device is controlled using I2C. Further information on the xCORE-200 Multichannel Audio Platform I2C bus can be found in §12.

9 USB Connectivity

The USB connectivity section consists of a USB A connector, USB B connector and a high-speed 3:1 switch to select between them.

The figure below shows the layout of the USB subsection:

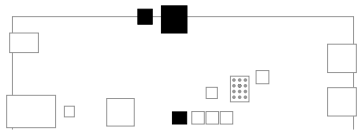

Figure 16: USB section

The USB signals are mapped onto the xCORE-200 device as shown in Figure 17

USB signal	xCORE GPIO	Port	Description
USB_D_N & P	See note		USB physical layer signals
USB_SEL0	X0D28	P4F0	Bit 0 of USB switch select signal
USB_SEL1	X0D29	P4F1	Bit 1 of USB switch select signal
VBUS_OUT_EN	X0D30	P4F2	Enable output onto VBUS

Figure 17: USB xCORE GPIO

Notes:

- The XE216 device incorporates a dedicated USB PHY device, so GPIO are not required

Two LEDs are provided to indicate the inverted status of USB select 0 and 1. The USB switch should be configured as shown in Figure 18

USB select	LED state	USB source	Description
0	Both on	NA	Sleep mode (DP, DN switch paths open
1	D28 ON	Reserved	
2	D29 ON	USB A connector	
3	Both off	USB B connector	

Figure 18: USB source selection

Notes:

5V is supplied to the USB A connector, from a local power supply, to provide VBUS to connected devices under the control of VBUS enable. This supply can be disabled by bringing the VBUS output enable low.

10 Ethernet Connectivity

Ethernet connectivity consists of a Gigabit Ethernet PHY and RJ45 connector with integrated magnetics. The figure below shows the layout of the Ethernet subsection:

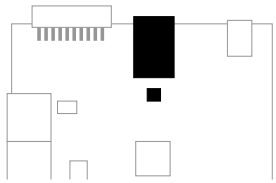

Figure 19: Gigabit Ethernet section

Three indivator LEDs are provided on the RJ45 connector:

- A yellow LED indicates activity
- A green LED indicates a Gigabit Ethernet connection
- An orange LED indicates a 10/100Mbps Ethernet connection

The RGMII signals are mapped onto the xCORE-200 device as shown in Figure 20

RGMII signal	xCORE GPIO	Description
TX_CLK	X1D26	
TX_CTL	X1D27	
RX_CLK	X1D28	
RX_CTL	X1D29	
RX0	X1D30	
RX1	X1D31	
RX2	X1D32	
RX3	X1D33	
TX0	X1D43	
TX1	X1D42	
TX2	X1D41	
TX3	X1D40	
INT	X1D03	
MDIO	X1D10	
MDC	X1D11	
ETH_RST_N	X1D02	

Figure 20: Ethernet xCORE GPIO

11 General purpose user interface

An array of 4*4 green LEDs, 3 buttons and a switch are provided for general purpose user interfacing. The LED array is driven by eight signals each controlling one of 4 rows and 4 columns.

The figure below shows the layout of the user interface subsection:

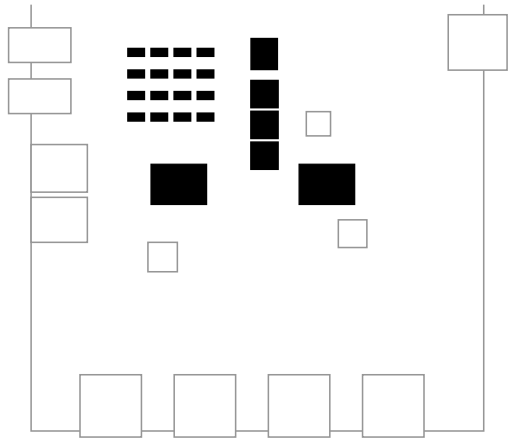

Figure 21: User interface components

The signal mapping of the user interface components is shown in Figure 22

UI signal	xCORE GPIO	Port	Description
LED_ROW_0	X1D14	P4C0	Row 0 LED driver control (active low)
LED_ROW_1	X1D15	P4C1	Row 1 LED driver control (active low)
LED_ROW_2	X1D20	P4C2	Row 2 LED driver control (active low)
LED_ROW_3	X1D21	P4C3	Row 3 LED driver control (active low)
LED_COL_0	X1D16	P4D0	Column 0 LED driver control (active low)
LED_COL_1	X1D17	P4D1	Column 1 LED driver control (active low)
LED_COL_2	X1D18	P4D2	Column 2 LED driver control (active low)
LED_COL_3	X1D19	P4D3	Column 3 LED driver control (active low)
BUTTON_1	X1D04	P4B0	Push button 1 (active low)
BUTTON_2	X1D05	P4B1	Push button 2 (active low)
BUTTON_3	X1D06	P4B2	Push button 3 (active low)
SWITCH_1	X1D07	P4B3	Common terminal of Slider switch 1

Figure 22: User interface GPIO

12 I2C bus address map

The address of the I2C bus on the xCORE-200 MC audio platform is shown in Figure 23

Figure 23: I2C address map

I2C address	Device
0x4C (0x99[r], 0x98[w])	CirrusLogic CS5368 Audio ADC
0x18 (0x31[r], 0x30[w])	CirrusLogic CS4384 Audio DAC
0x4E (0x9D[r], 0x9C[w])	CirrusLogic CS2100 PLL

13 xSYS Debug

A standard XMOS xSYS interface is provided to allow host debug of the board via JTAG.

An XTAG debug adapter can be plugged into this port to allow running/debugging code, programming the FLASH memory and selection of boot mode. A 20-way IDC header is used as the physical connector and the pinout of this is shown below:

Figure 24: XSYS Connector Pinout

XSYS signal	xCORE GPIO	Header pin	Description
TMS	See note	7	JTAG Test Mode Select.
TCK	See note	9	JTAG Test Clock.
TDI	See note	5	JTAG Test Data In. From debug adapter to XS1-U8.
TDO	See note	13	JTAG Test Data Out. From XS1-U8 to debug adapter.
RST_N	See note	15	System Reset. Active low, resets XS1-U8 device
GND		4, 8, 12, 16, 20	Ground.
XL_UP1	X0D43	6	XMOS link, uplink bit 1
XL_UP0	X0D42	10	XMOS link, uplink bit 0
XL_DN1	X0D40	14	XMOS link, downlink bit 1
XL_DN0	X0D41	18	XMOS link, downlink bit 0

Notes:

- JTAG connections occupy dedicated connections

On power on, the XE216 device boots from the on-board flash memory. With the xTAG connected, the XE216 can be reset and then booted from a program on the host PC.

14 QSPI Flash

xCORE-200 Multichannel Audio Platform provides 2Mbytes of Quad Serial Peripheral Interface (QSPI) FLASH memory, which is interfaced by the GPIO connections shown in Figure 25:

QSPI connection	Pin	Port
SPI_CS	X0D01	P1B
QSP_D0	X0D04	P4B0
QSP_D1	X0D05	P4B1
QSP_D2	X0D06	P4B2
QSP_D3	X0D07	P4B3
SPI_CLK	X0D10	P1C

Figure 25: QSPI Flash

The xTIMEcomposer tools include the xFLASH utility for programming compiled programs into the flash memory. xCORE-200 Multichannel Audio Platform designs may also access the FLASH memory at run-time by interfacing with the above pins.

15 Operating requirements

A USB 2.0 high-speed compliant cable of less than 3m in length should be used when operating the xCORE-200 Multichannel Audio Platform. XMOS cannot guarantee correct operation of the xCORE-200 Multichannel Audio Platform should any other cable be used.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the xCORE-200 Multichannel Audio Platform with appropriate ESD precautions in place.

16 Dimensions

The xCORE-200 Multichannel Audio Platform dimensions are 180x110mm. The mounting holes are 2mm in diameter.

17 xCORE-200 Multichannel Audio Platform Portmap

The table below provides a full description of the port-pin mappings described throughout this document for the XK-AUDIO-216-MC-AB board.

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X0D00	$1A^0$					PLL_SYNC
X0D01	$1B^0$					SPI_CS
X0D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	I2C_SCL
X0D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	I2C_SDA
X0D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	QSPI_D0
X0D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	QSPI_D1
X0D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	QSPI_D2
X0D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	QSPI_D3
X0D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	
X0D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	
X0D10	$1C^0$					SPI_CLK
X0D11	$1D^0$					COAX_TX
X0D12	$1E^0$					OPT_TX
X0D13	$1F^0$					MCLK_XCORE
X0D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	
X0D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	OVERFLOW
X0D16		$4D^0$	$8B^2$	$16A^{10}$		BUTTON_1
X0D17		$4D^1$	$8B^3$	$16A^{11}$		BUTTON_2
X0D18		$4D^2$	$8B^4$	$16A^{12}$		BUTTON_3
X0D19		$4D^3$	$8B^5$	$16A^{13}$		SWITCH_1
X0D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	
X0D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	
X0D22	$1G^0$					LRCLK
X0D23	$1H^0$					SCLK
X0D24	$1I^0$					xSDIO1
X0D25	$1J^0$					xSDIO2
X0D26		$4E^0$	$8C^0$	$16B^0$		DSD_MODE
X0D27		$4E^1$	$8C^1$	$16B^1$		DAC_RST_N
X0D28		$4F^0$	$8C^2$	$16B^2$		USB_SEL0
X0D29		$4F^1$	$8C^3$	$16B^3$		USB_SEL1
X0D30		$4F^2$	$8C^4$	$16B^4$		VBUS_OUT_EN
X0D31		$4F^3$	$8C^5$	$16B^5$		PLL_SELECT
X0D32		$4E^2$	$8C^6$	$16B^6$		ADC_RST_N
X0D33		$4E^3$	$8C^7$	$16B^7$		MCLK_FSEL
X0D34	$1K^0$					xSDIO3
X0D35	$1L^0$					xSDIO4
X0D36	$1M^0$		$8D^0$	$16B^8$		xDAC_SD1
X0D37	$1N^0$		$8D^1$	$16B^9$		xDAC_SD2
X0D38	$1O^0$		$8D^2$	$16B^{10}$		xDAC_SD3
X0D39	$1P^0$		$8D^3$	$16B^{11}$		xDAC_SD4
X0D40			$8D^4$	$16B^{12}$		XL_DN1
X0D41			$8D^5$	$16B^{13}$		XL_DN0
X0D42			$8D^6$	$16B^{14}$		XL_UP0
X0D43			$8D^7$	$16B^{15}$		XL_UP1

Figure 26: xCORE-200 Multichannel Audio Platform Portmap

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X1D00	$1A^0$					
X1D01	$1B^0$					
X1D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	ETH_RST_N
X1D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	ETH_INT
X1D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	BUTTON_1
X1D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	BUTTON_2
X1D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	BUTTON_3
X1D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	SWITCH_1
X1D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	
X1D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	
X1D10	$1C^0$					MDIO
X1D11	$1D^0$					MDC
X1D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	LED_ROW_0
X1D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	LED_ROW_1
X1D16		$4D^0$	$8B^2$	$16A^{10}$		LED_COL_0
X1D17		$4D^1$	$8B^3$	$16A^{11}$		LED_COL_1
X1D18		$4D^2$	$8B^4$	$16A^{12}$		LED_COL_2
X1D19		$4D^3$	$8B^5$	$16A^{13}$		LED_COL_3
X1D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	LED_ROW_2
X1D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	LED_ROW_3
X1D26		$4E^0$	$8C^0$	$16B^0$		ETH_TX_CLK
X1D27		$4E^1$	$8C^1$	$16B^1$		ETH_TX_CTL
X1D28		$4F^0$	$8C^2$	$16B^2$		ETH_RX_CLK
X1D29		$4F^1$	$8C^3$	$16B^3$		ETH_RX_CTL
X1D30		$4F^2$	$8C^4$	$16B^4$		ETH_RX0
X1D31		$4F^3$	$8C^5$	$16B^5$		ETH_RX1
X1D32		$4E^2$	$8C^6$	$16B^6$		ETH_RX2
X1D33		$4E^3$	$8C^7$	$16B^7$		ETH_RX3
X1D35	$1L^0$					MCLK
X1D36	$1M^0$		$8D^0$	$16B^8$		MIDI_RX
X1D37	$1N^0$		$8D^1$	$16B^9$		MIDI_TX
X1D38	$1O^0$		$8D^2$	$16B^{10}$		OPT_RX
X1D39	$1P^0$		$8D^3$	$16B^{11}$		COAX_RX
X1D40			$8D^4$	$16B^{12}$		ETH_TX3
X1D41			$8D^5$	$16B^{13}$		ETH_TX2
X1D42			$8D^6$	$16B^{14}$		ETH_TX1
X1D43			$8D^7$	$16B^{15}$		ETH_TX0

Figure 27: xCORE-200 Multichannel Audio Platform Portmap

18 xCORE-200 Multichannel Audio Platform schematics

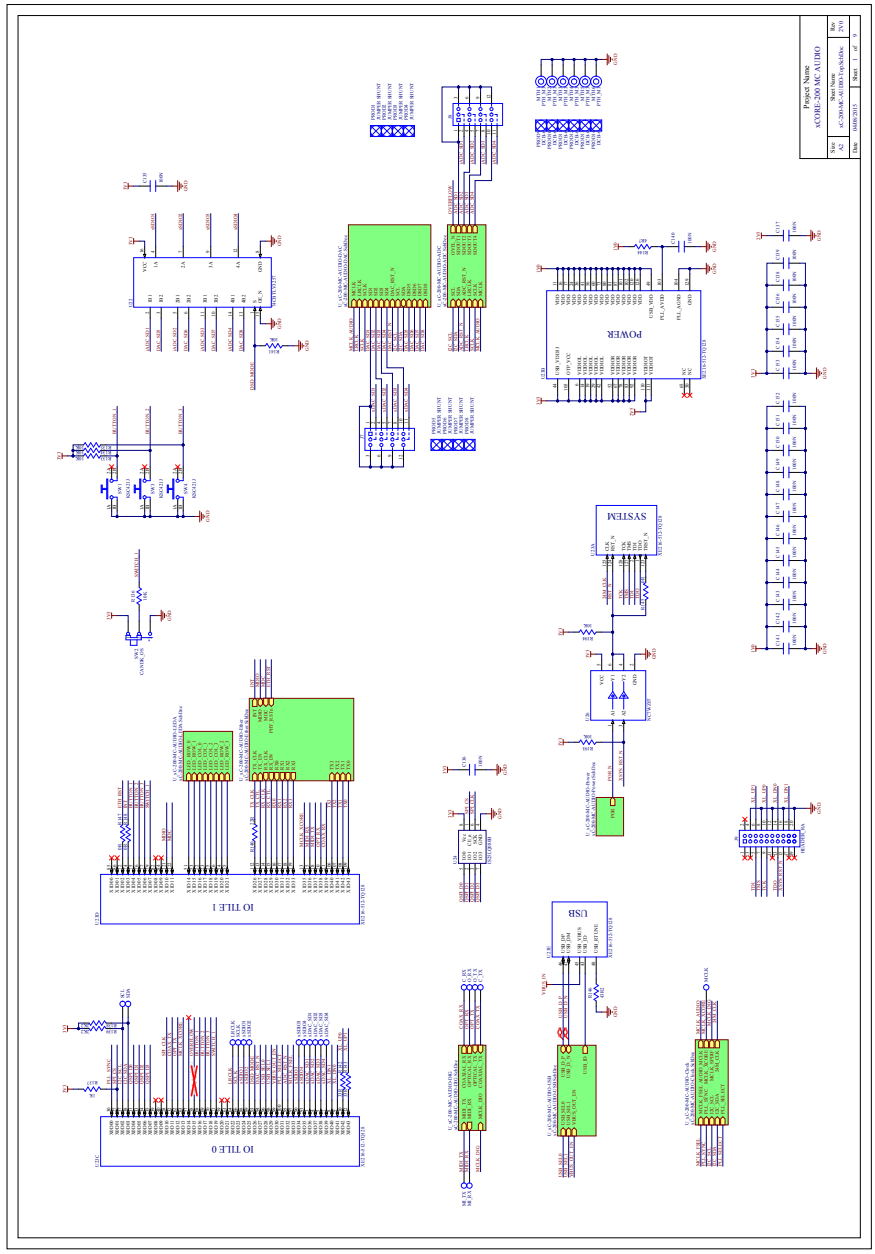

Figure 28: xCORE-200 Multichannel Audio Platform schematic (1 of 9)

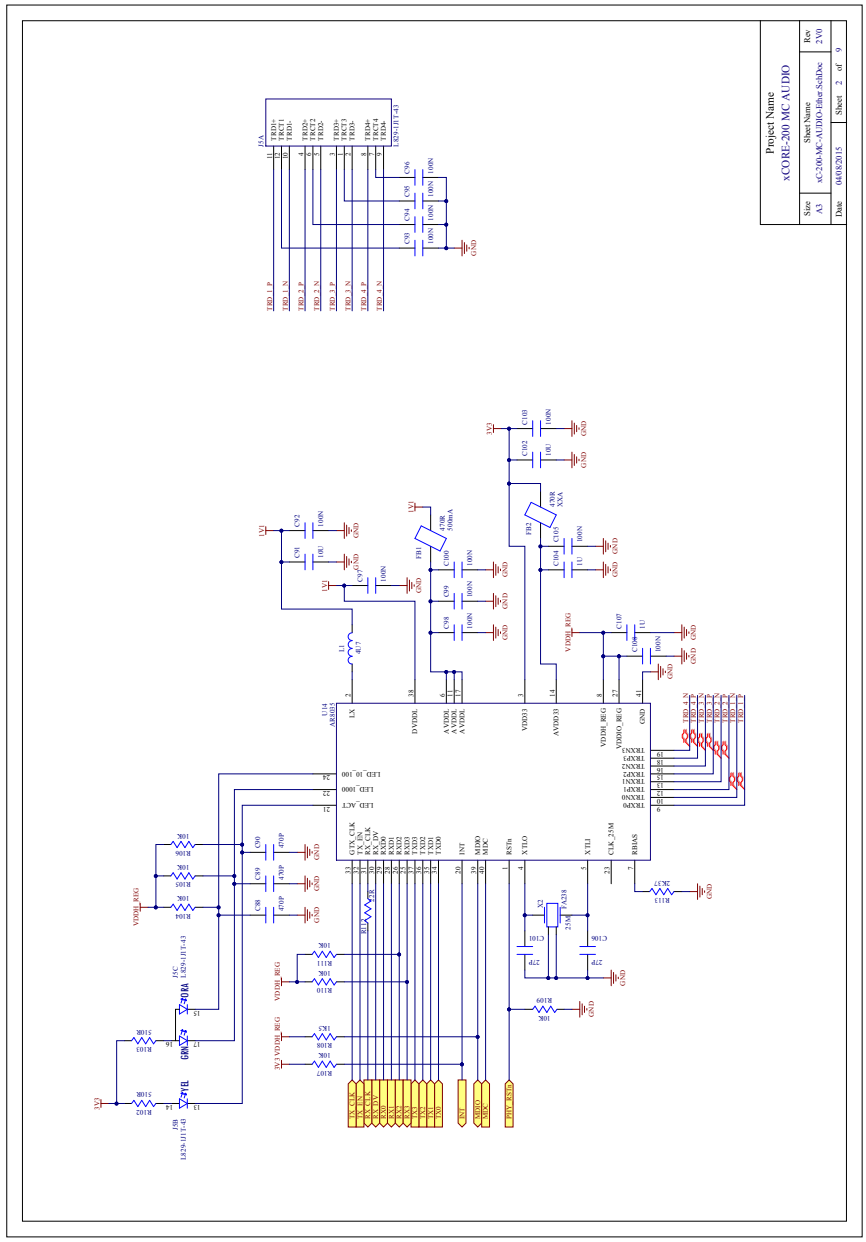

Figure 29: xCORE-200 Multichannel Audio Platform schematic (2 of 9)

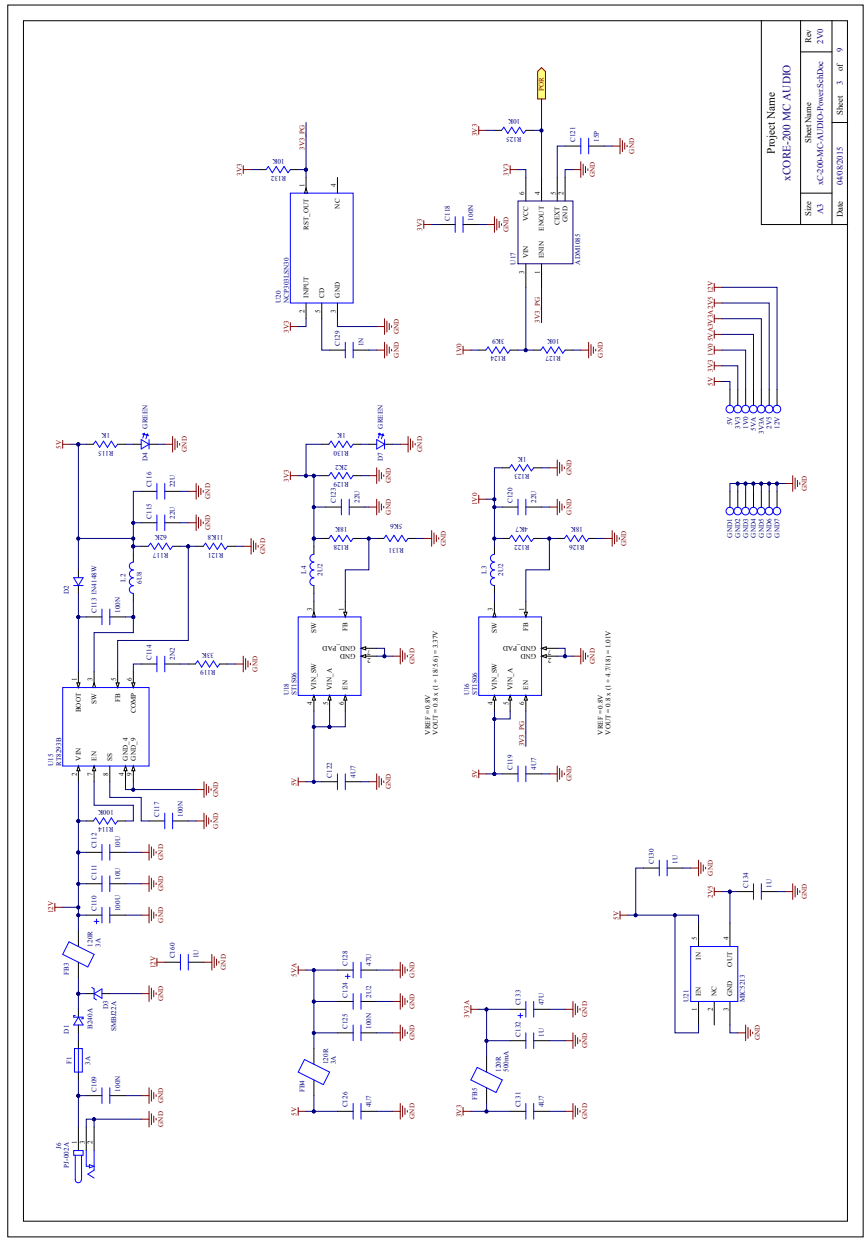

Figure 30: xCORE-200 Multichannel Audio Platform schematic (3 of 9)

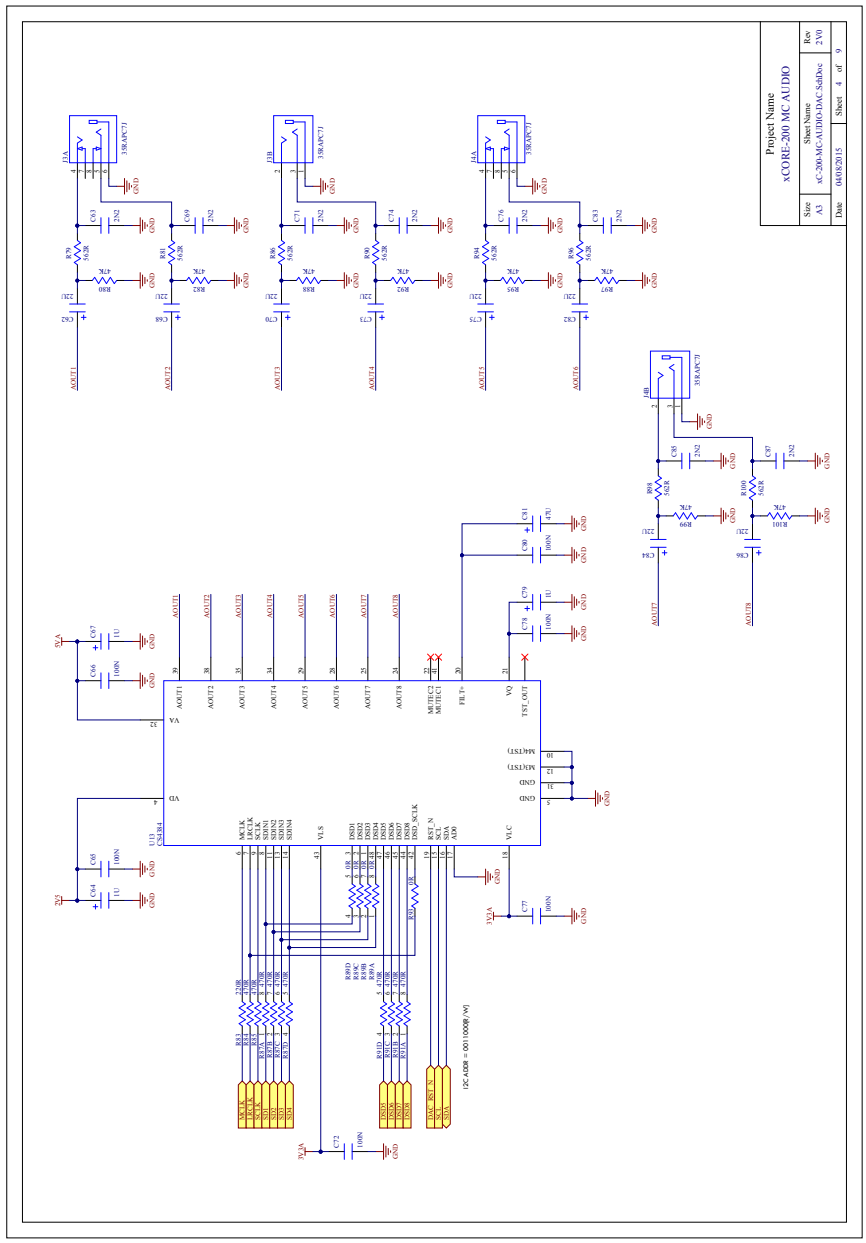

Figure 31: xCORE-200 Multichannel Audio Platform schematic (4 of 9)

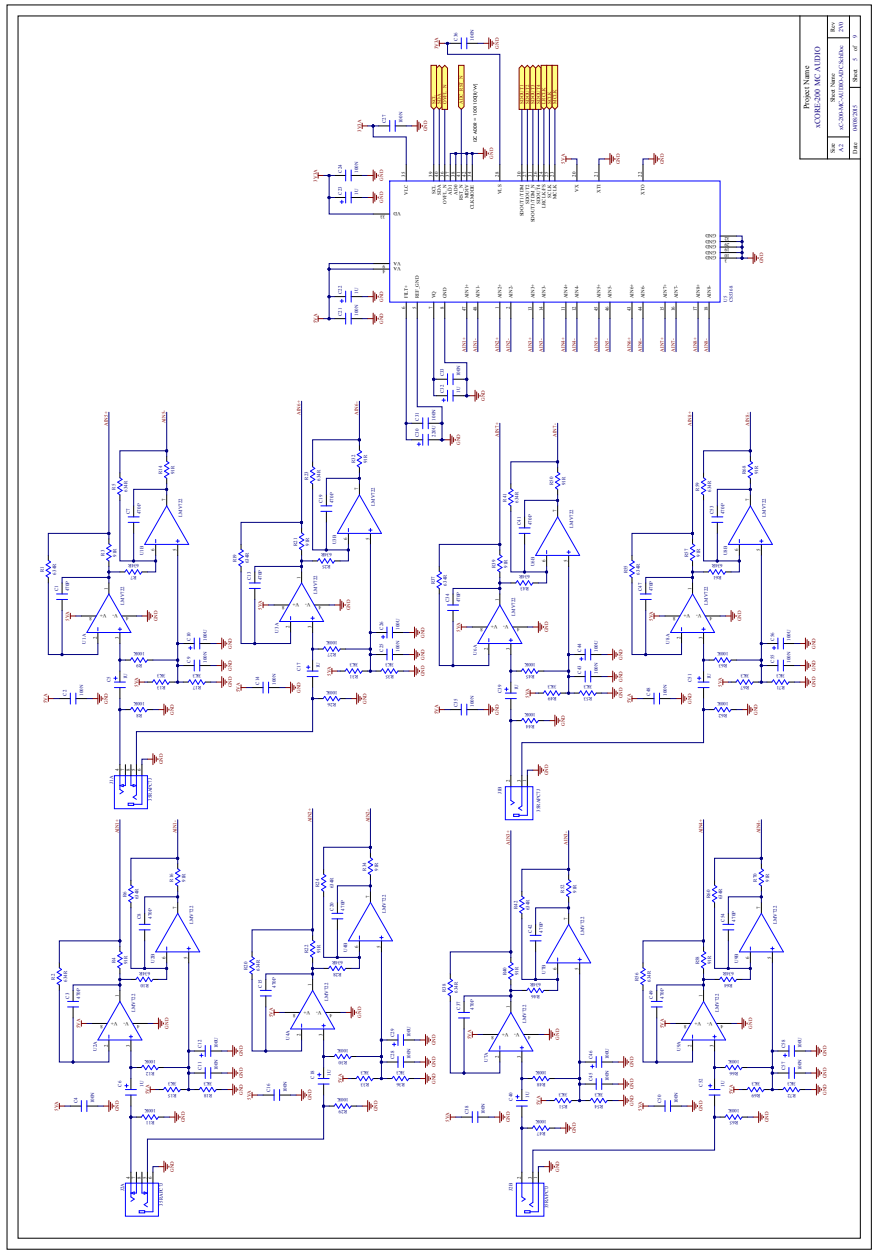

Figure 32: xCORE-200 Multichannel Audio Platform schematic (5 of 9)

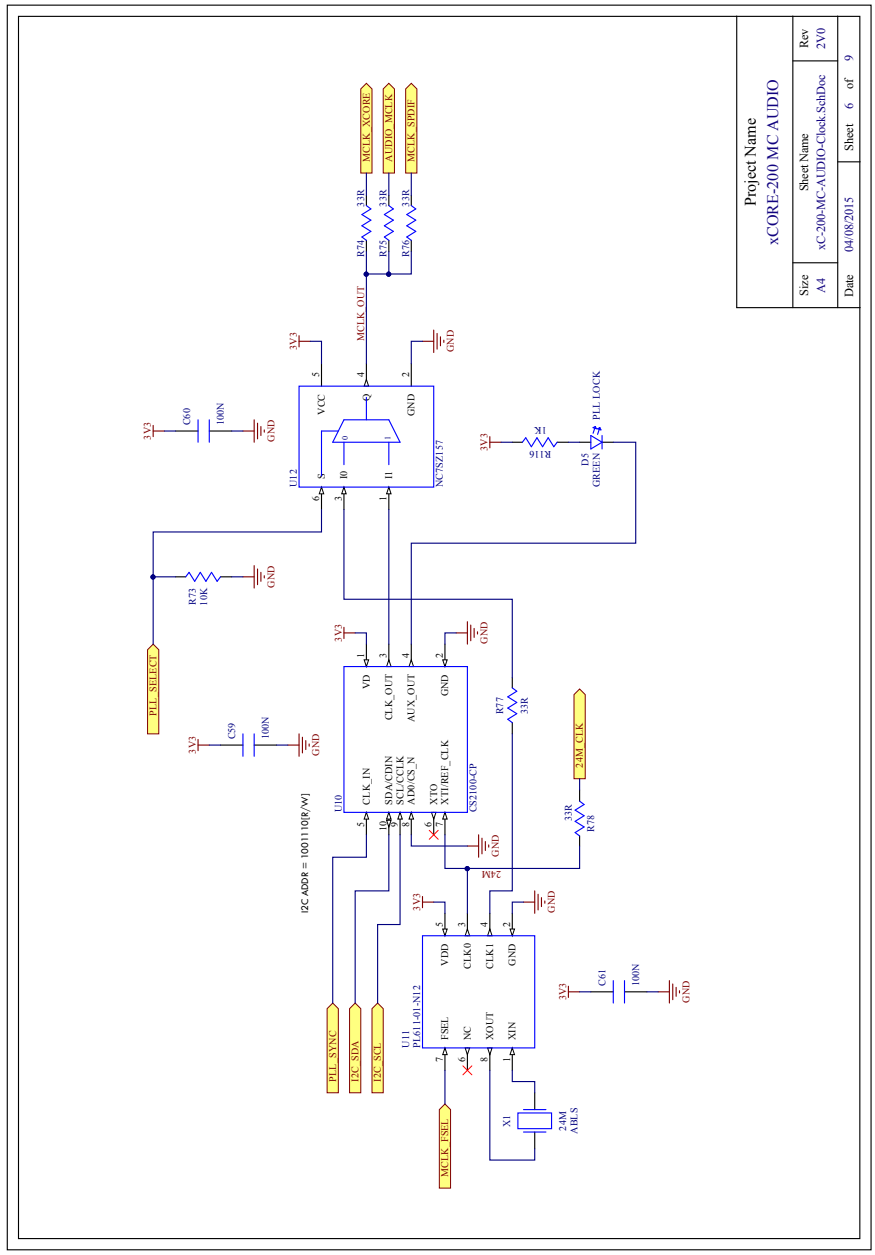

Figure 33: xCORE-200 Multichannel Audio Platform schematic (6 of 9)

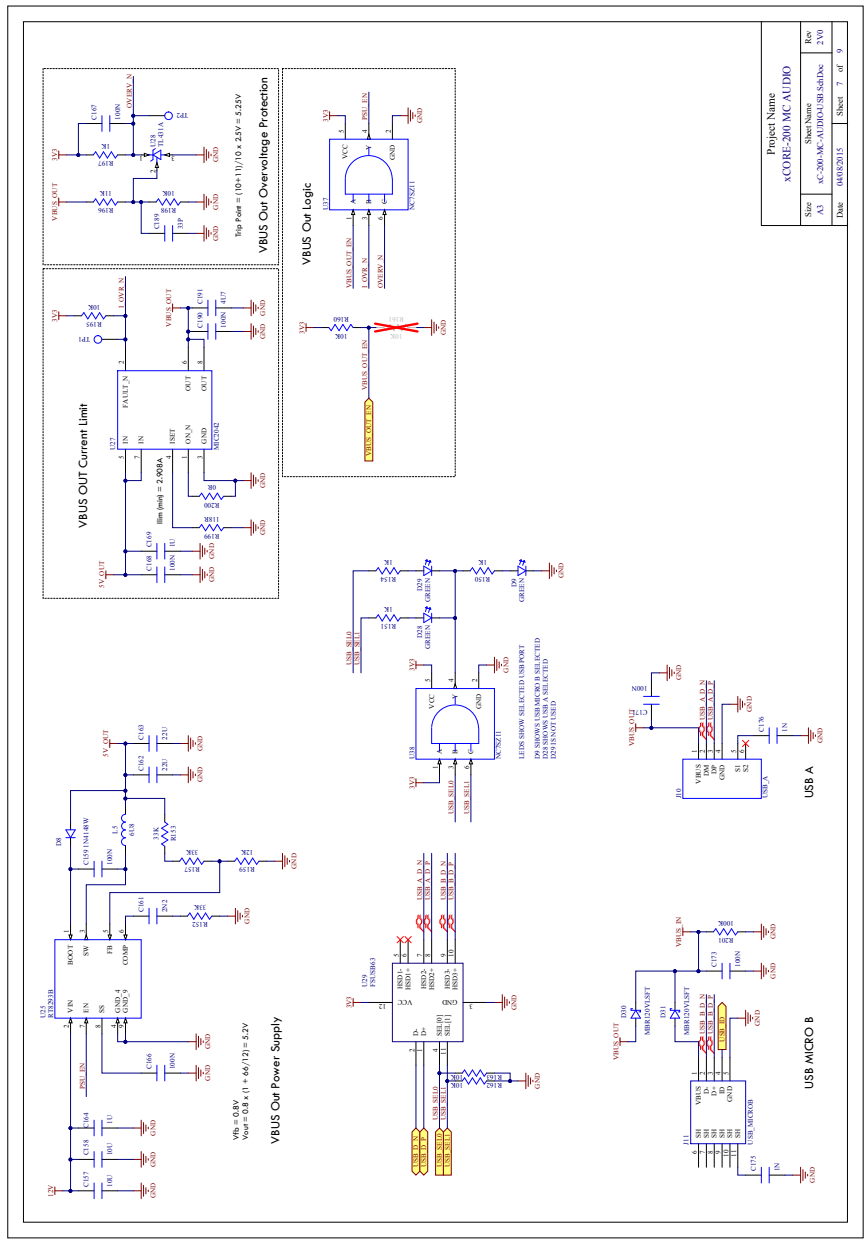

Figure 34: xCORE-200 Multichannel Audio Platform schematic (7 of 9)

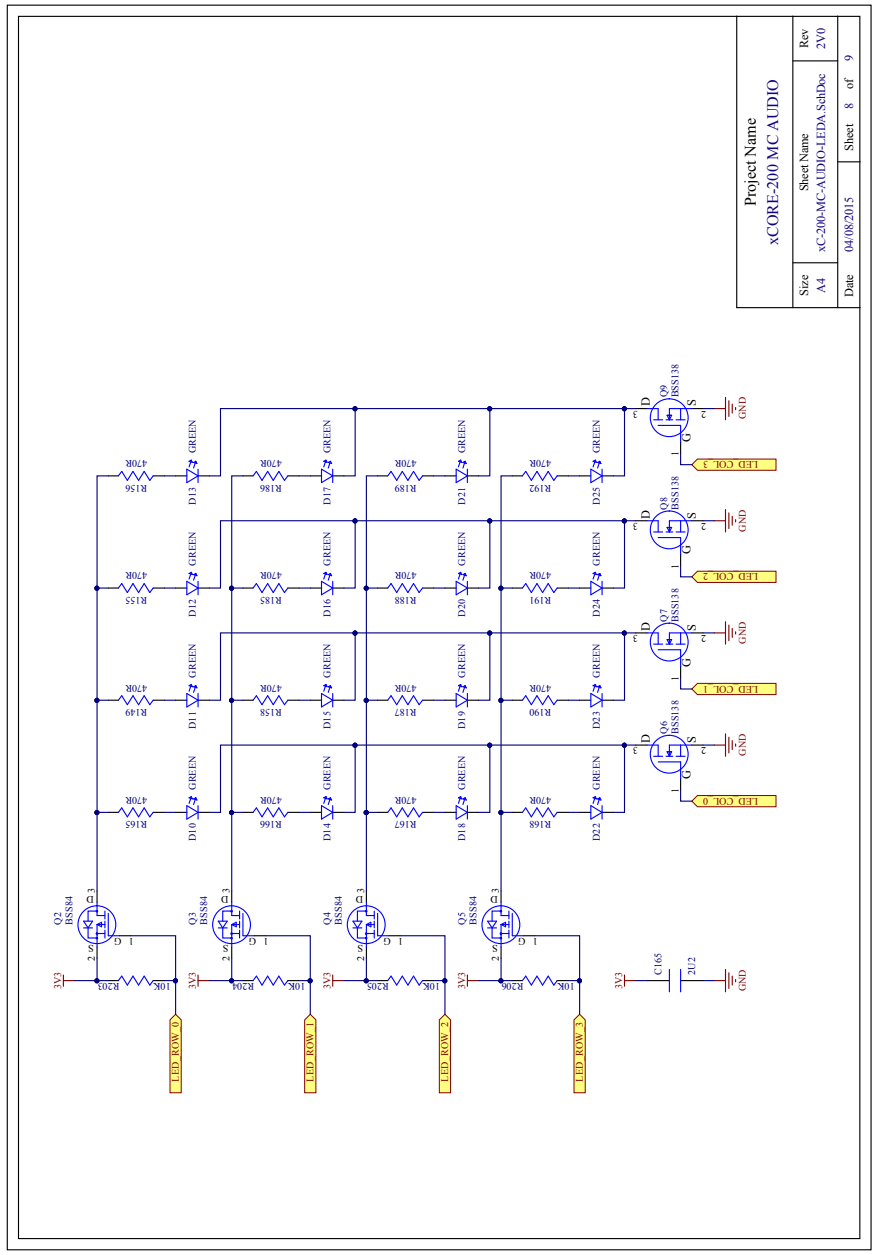

Figure 35: xCORE-200 Multichannel Audio Platform schematic (8 of 9)

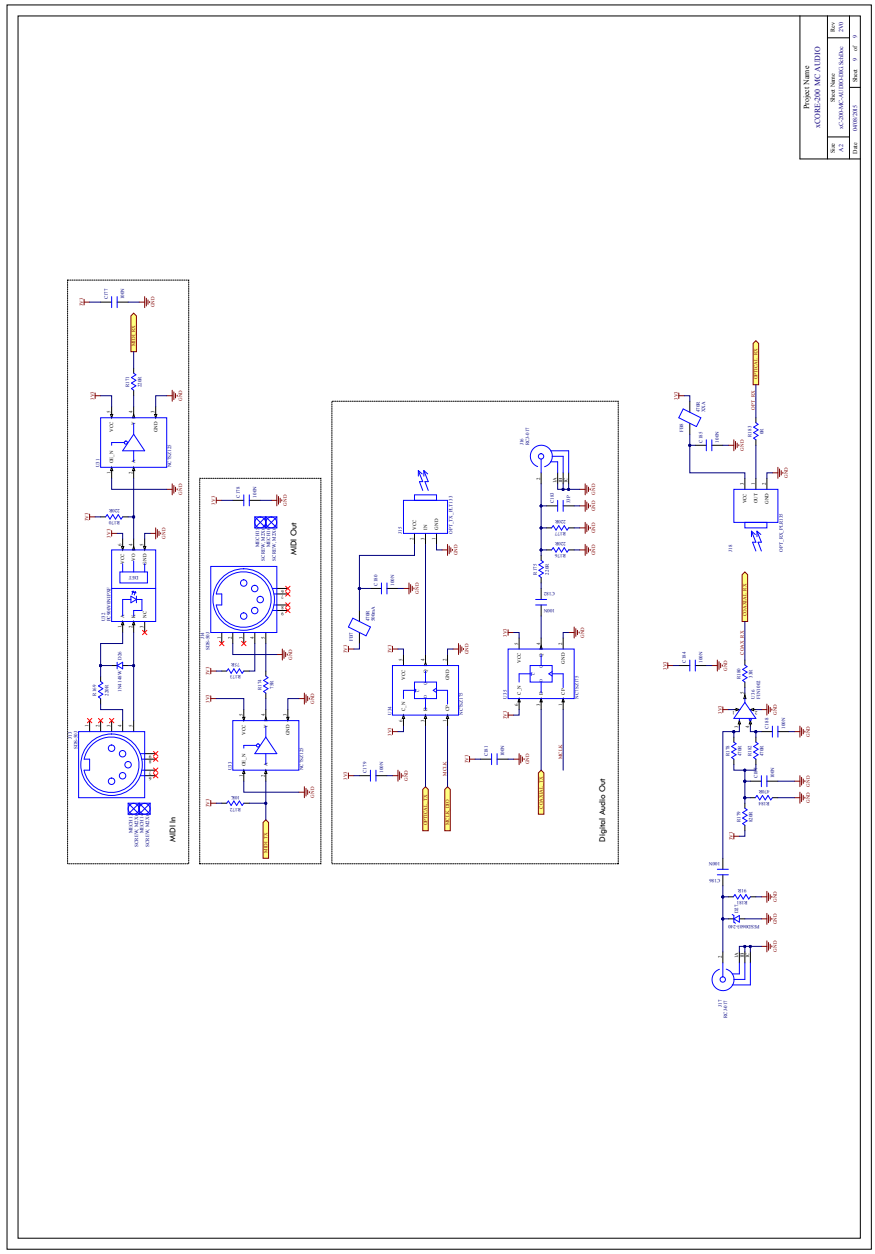

Figure 36: xCORE-200 Multichannel Audio Platform schematic (9 of 9)

19 RoHS and REACH

The xCORE-200 Multichannel Audio Platform complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The xCORE-200 Multichannel Audio Platform is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.

20 Version history

Date	Description
2015/5/14	First board release, 2v0 hardware