XS1-L Link Performance and Design Guidelines

Version 1.1

XMOS

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1 Overview

This document is intended to assist designers of systems incorporating multiple XMOS XS1 family devices, using the propitiatory XMOS Link architecture to connect the devices together. The following aspects of the system design are covered in this document:

- What size parts do you need (L1-64/L1-128/L2-124)?
- How many links and what type (2w/5w) do you need?
- What will the topology be like?
- Which links to choose so that the whole system boots from one SPI flash?

XMOS Links have two operating modes, 2 wire (serial mode) and 5 wire (fast mode). A 2 wire (2w) link has 2 signal wires in each direction (RX/TX); a 5 wire (5w) link has 5 signal wires in each direction. A single transition on one link wire transmits one symbol in that direction in 2w mode, and two symbols in 5w mode. Connection is required in both directions, because the protocol is handshaked.

Groups of symbols are routed through the interconnect system as packets comprising a whole number of bytes with some additional control information and a small amount of control overhead, such as headers with routing information, and 'end of packet' (EOP) markers. A byte of data is transferred as 10 symbols (serial mode) or 4 symbols (fast mode).

2 Inter-Symbol Delay

The time between transmitting symbols (the inter-symbol delay) must be set to ensure signal transitions are sufficiently spaced out to be safely acquired at the receiver. The maximum speed of a link is determined mainly by the variability in transition timing between the wires of the link. Variations in the position of transitions are affected by:

- Process, temperature and dynamic voltage variability on the XS1 device.
- Pad delay variability, especially the difference in propagation delays of rising and falling transitions through the XS1 pads.
- Line delay variability arising from PCB design and re-buffering.

The inter-symbol delay or *symbol time* (T_{symbol}) is a multiple of the transmitter's switch clock cycle time. Lab testing has indicated that a symbol time of 7.5ns should be achievable under all the scenarios described in *Deployment Scenarios* Section 9.

3 Data Rates

The serial (2w) link uses 10 symbols per byte, and the fast (5w) link uses 4 symbols per byte.

The raw data rate can the be calculated based on the symbol time as follows:

XMOS serial link bandwidth (bytes/second) = $^1/_{10}\ T_{symbol}$
XMOS fast link bandwidth (bytes/second) = $^1/_4\ T_{symbol}$

Each packet sent over an XMOS Link includes a 3 byte or 1 byte header, which is user configurable depending on the size of the network. For small networks of a few chips, 1 byte headers should suffice[1]. The end of each packet has an EOP marker. Finally, hardware generated credit messages are employed to manage throughput. Taking into account all these overheads and assuming an average packet size of 32 bytes with a symbol time of 7.5ns yields the following effective data rates per link:

Link Mode	Header	**Data Rate**
2w	1 byte	11.4 MBytes/sec
5w	1 byte	30.5 MBytes/sec

4 Link Resources

XS1 parts have the following link resources available, each of which can be employed in 5 wire or 2 wire mode. They are called X0LA, X0LB, X0LC, X0LD, and X1LA, X1LB for the dual-core device.

Device	**XMOS Links**			
XS1-L1-64LQFP	X0LA	X0LB		
XS1-L1-128TQFP	X0LA	X0LB	X0LC	X0LD
XS1-L1-124QFN	X0LA	X0LB	X1LA	X1LB

The package pins are shared between links and I/Os—when a link is enabled, I/Os that use these pins are disabled. Please refer to product datasheets for a complete map of I/Os and links.

[1] 3 byte headers can be used to provide a slightly faster data rate compared to 1 byte headers, but this is generally only an issue for large multiple-chip networks. Information on developing such networks is beyond the scope of this document, please contact XMOS for further details.

5 Booting over XMOS Links

Any XS1 family device may be configured to boot over its X0LB link. Systems comprised of a single master device that boots from a SPI flash can have additional slaved devices that are subsequently booted over the master device XMOS Links including slave devices that are only connected to the master through intervening slave devices.

The XMOS software tools provide the option to describe your system topology in terms of connected XS1 devices and SPI flash devices. The tools handle all the required system switch setup and boot strapping.

6 XS1-L1 System Topologies

Figure 1 shows the connection of two XS1-L1-64LQFP devices. The master boots from SPI flash and then boots the slave via X0LB in 2w mode. Following boot, the link may be reconfigured in 5w mode to offer an inter-chip bandwidth of up to 30.5MBytes/second.

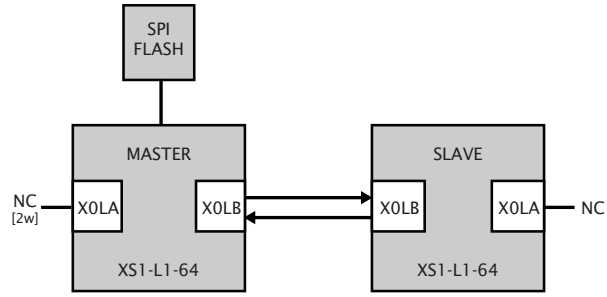

Figure 1: XS1-L1-64LQFP two chip system

Links marked NC in Figure 1 are not required by the system topology. The I/O pins that overlap these XMOS Link can be used for other purposes.

Figure 2 shows the connection of two XS1-L1-128TQFP devices. The master boots from SPI flash and then boots the slave via X0LB. The remaining links X0LC and X0LD (together with X0LB) offer an interchip bandwidth of 91.5 Mbytes/second.

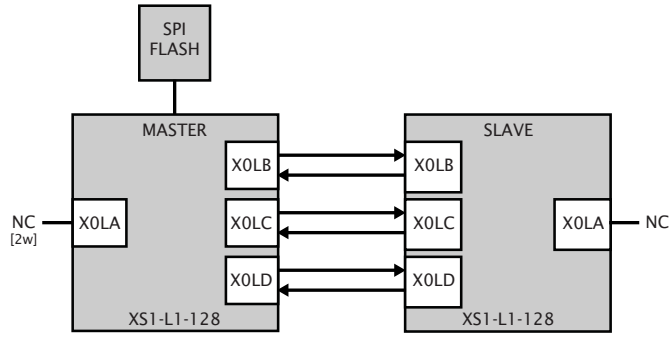

Figure 2: XS1-L1-128TQFP two chip system

Figure 3 and Figure 4 show two possible ways of interconnecting three XS1-L1-128TQFP devices. The devices are connected in a 2D line topology, with the master device at one end or in the centre.

In Figure 3 (the master is located at one end of the line) the slave at the far end is booted by routing the data it needs to boot via the system switch of the middle device. This will be transparent to software running on the middle device, as will subsequent messages between the two devices at the end of the line after the whole system has booted and is operating.

Both configurations offer 61MBytes/second between each adjacent node in the network, except configuration 2's master and left slave, where there is only one 5w link providing 30.5Mbytes/sec.

Note that links are not required to match (for example X0LA on one device can connect to X0LB on another).

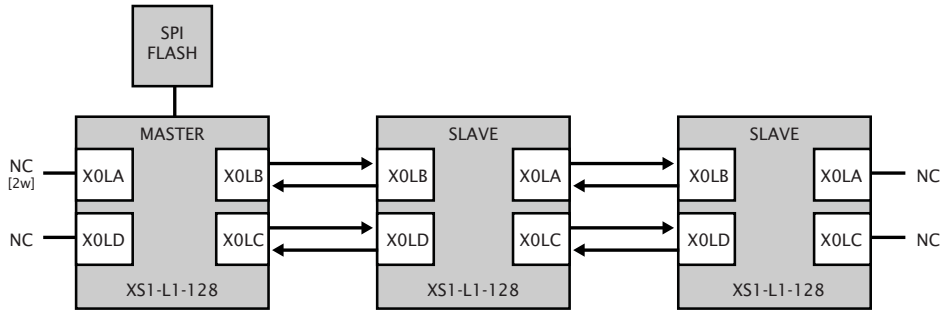

Figure 3: XS1-L1-128TQFP three chip system 1

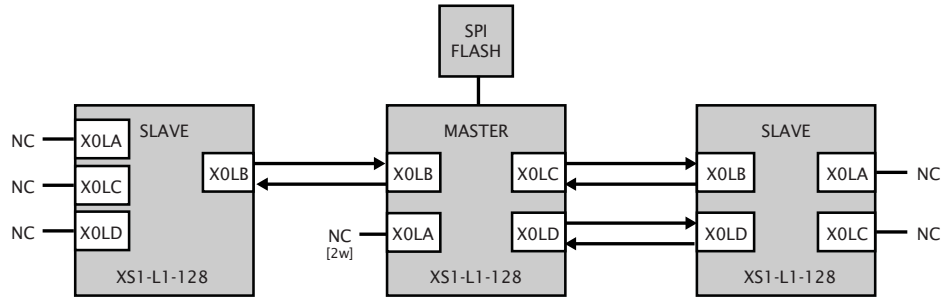

Figure 4: XS1-L1-128TQFP three chip system 2

Note that in all the system topologies outlined above the key constraints are:

1. The master which boots from SPI cannot use X0LA in 5 wire mode (because some pins are the SPI I/O pins).
2. All slave devices are connected in the master-ward direction using X0LB.
3. Subject to constraints 1 and 2, remaining free XMOS Links on devices in the system may be connected as required but must not be connected so as to form a loop topology. For example, in Figure 3 the device on the right must not be connected back to the master.

7 XS1-L2 System Topologies

The XS1-L2 is a multi-chip module containing 2 XS1 dies interconnected in-package by 4 dedicated XMOS Links which are not pinned out on the XS1-L1 device family. The L2 device thus offers 122MBytes/second inter-core bandwidth within the L2 module. It also offers externally (see table—Section 4) two links from each device in the module.

Topologies for multiple L2 devices (or a mix of L2 and L1 devices) is similar to the L1 only topologies, with the exception that the slave die within the L2 module is always booted by the master die within the same module. Therefore to boot an L2 device as a slave over XMOS Links, link X0LB on the master core must be used. Any free outgoing link can then be used to boot further downstream L1 or L2 devices.

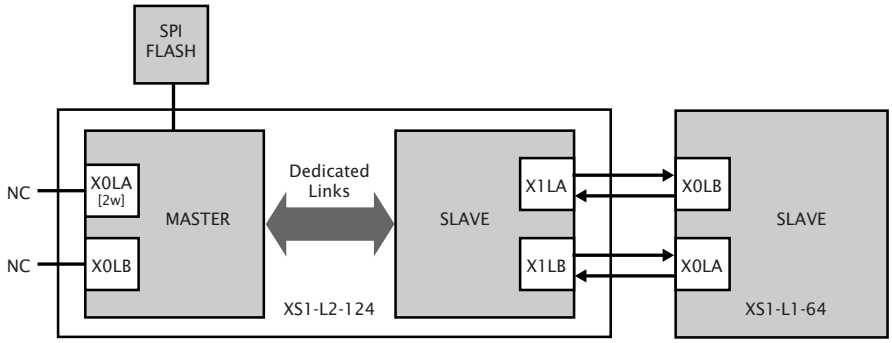

Figure 5: Mixed XS1-L1 and XS1-L2 system 1

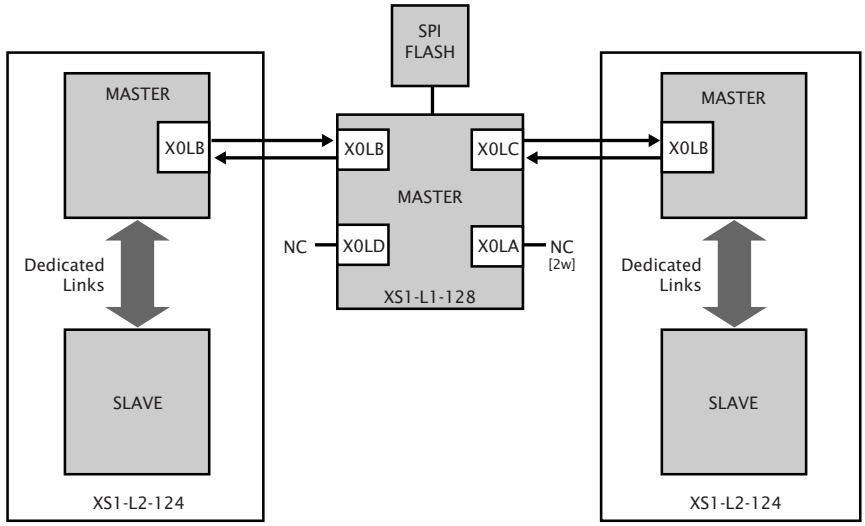

Figure 6: Mixed XS1-L1 and XS1-L2 system 2

8 Layout Guidelines

8.1 Link Compatability

The XMOS Links between the XS1-G and XS1-L family are not compatible and cannot be connected together.

8.2 Crosstalk and Noise

Because XMOS Links are a transition-based protocol rather than a level-based protocol, they are vulnerable to noise via crosstalk or EMI. Accordingly XMOS Links should be designed to minimize noise:

- Do not route the signals closely in parallel for large distances. The traces need separating out to minimize cross-talk between the lines.
- Do not route the signals close to noisey items on the PCB (such as switch-mode power supplies and clocks).
- Try not to route the XMOS Link over splits in the ground plane, as the return ground currents can cause cross-talk.
- If the traces are going over long distances, use low voltage differential signalling transceivers (LVDS) at each of the link to make the links immune to common-mode interference (for example DS90LV049 as used in the XDK) and improve the achievable symbol rate be utilized.

8.3 Pulldown Resistors

When XMOS Links are enabled, the wires should be logic low. Weak internal pull downs are active on the XMOS Link pins before they are enabled. These pull downs cannot be relied upon to pull down long traces with high capacitance. Circuit designers should apply external pull down resistors on such tracks.

9 Deployment Scenarios

The following XMOS Link examples all operate error free with an inter symbol delay of 7.5ns.

L2 inter-core XMOS Links – The XS1 L2 device uses 4 XMOS Links connected in 5w fast mode between the two XCores in the package.

2w link with 150mm FPC Flexible Ribbon Cable – Serial (2w) Link utilizing 4 signal (2 per link direction) and 2 ground wires, with single ended drivers (for example 74AUP2G17) located at driving (TX) pins.

2w link with 150mm FPC Flexible Ribbon Cable and LVDS Transceivers – Serial (2w) Link utilizing 8 signal (2 differential pairs per link direction) and 6 ground wires, with LVDS transceivers (for example DS90LV049) located at each end of each link wire.

2w link with 1000mm RJ45 double shielded cables and LVDS Transceivers – Serial (2w) Link utilizing 8 signal (2 differential pairs per link direction) and 2 ground wires, with LVDS transceivers (for example DS90LV049) located at each end of each link wire.

5w and 2w Link with up to 100mm of PCB Track – Link with 33R series terminating resistors close to the TX sides of each wire, using no driver chips.

10 EMI

XMOS Links are awaiting EMI qualification. Please contact XMOS if further discussion of noise immunity is required.

XMOS also advises customers to have the noise immunity of their own particular design employing XMOS Links tested in the appropriate laboratory environment.

11 Document History

Date	Release	Comment
2010-02-22	1.0	First release
2010-03-16	1.1	Amended Layout Guidelines section Clarified use of NC links

Disclaimer