XS1 Link Performance and Design Guidelines

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This document is intended to assist designers of systems incorporating multiple XMOS XS1 family devices. XS1 devices are connected together using *XMOS links* and *switches*, together comprising the XMOS *xCONNECT* interconnect. This document focuses on the physical aspects of links; all other aspects are discussed in detail in the *xCONNECT architecture*[1] documentation.

XMOS links use a transition based signalling scheme. A single transition on a wire transmits one symbol. XMOS links have two operating modes, 2 wire (serial mode) and 5 wire (fast mode).

- A 2-wire (2w) link has two signal wires in each direction. A data byte is transmitted as a series of ten transitions on wire 0 and/or 1.
- A 5-wire (5w) link has five signal wires in each direction. A data byte is transmitted as a sequence of four transitions on the 5 wires.

Besides data bytes, control information can be transmitted, for example to transmit an 'END' token signalling the end of a packet.

This document applies to the XS1-L, XS1-U, and XS1-A families. XS1-G links are not compatible and are discussed in a separate document.

1 Inter-Symbol Delay

The time between transmitting symbols (the inter-symbol delay) governs the speed at which the link operates. The shorter the inter-symbol delay, the faster the link operates. However, if the inter-symbol delay is too short, then symbols may not arrive at the receiver intact, or in-order. If two symbols are transmitted on the same wire in quick succession, then the resulting pulse may be too short to physically

[1] http://www.xmos.com/published/xconnect-architecture

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arrive on the other side. If two symbols are transmitted in quick succession on two different wires, then the last transition may overtake the first transition between the transmitter and receiver. Both will cause packet corruption, and should be avoided by design.

Symbol integrity may be affected by:

- Process, temperature and dynamic voltage variability on the XS1 device.
- Pad delay variability.
- The difference in propagation delays of rising and falling transitions through the pads.
- Line delay variability arising from PCB design.

The *inter-symbol delay* is measured in terms of the number of clock ticks of the switch that is transmitting the data. Depending on the deployment scenario, inter-symbol delays of as little as 4 ns will work reliably. In addition to the inter-symbol delay, the *inter-token delay* can be set. This is normally set to the same delay as the inter-symbol delay, but can be set to a larger value for connecting to devices that may require a delay between tokens, or for debugging a link.

2 Data Rates

The serial (2w) link uses 10 symbols per token, and the fast (5w) link uses 4 symbols per token. Hence the token-rate is one-tenth of the symbol rate in 2w mode and one-fourth of the symbol rate in 5w mode. To convert this token-rate to a byte-rate, you need to compensate for the time taken to send credit tokens; for every 16 tokens sent from Tx to Rx, Rx has to send one *credit token* back to Tx. This credit token will be interspersed with the traffic in the reverse direction. So, maximum data rates depend on the link mode, the inter symbol delay, and one whether maximum traffic is travelling in just one direction or both directions simultaneously:

LinkMode	Delay	Data rate in Mbyte/sec	
		two-way	one-way
2w	7.5 ns	12.5	13.3
5w	7.5 ns	31	33.3
2w	5 ns	18	20
5w	5 ns	46	50

When data is sent as packets, a header is required to route the packet, and an END token is required to terminate the packet. Depending on the size of the system, this occupies two or four tokens. This overhead should be taken into account when computing the maximum throughput for small packets.

3 Link Resources

The number of links that are bonded out on a chip depend on the package. Some packages have as little as two links, some as many as four links. The package pins are shared between links and I/Os—when a link is enabled, I/Os that use these pins are disabled. The product datasheets contain a complete map of I/Os and links.

4 Booting over XMOS links

Any XS1 family device may be configured to boot over its X0LB link. Systems comprised of a single master device that boots from a SPI flash can have additional slave devices that are subsequently booted by the master device xCONNECT links including slave devices that are only connected to the master through other slave devices.

The xTIMEcomposer tools provide the option to describe your system topology in terms of connected XS1 devices and SPI flash devices. The tools handle all the required system switch setup and boot strapping.

5 XS1 System Topologies

Figure 1 shows the connection of two XS1-L8A-64-64LQFP devices. The master boots from SPI flash and then boots the slave via X0LB in 2w mode. Following boot, the link may be reconfigured in 5w mode to offer an inter-chip bandwidth of up to 30.5Mbits/second.

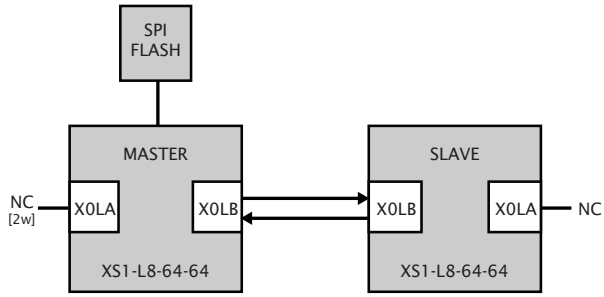

Figure 1: XS1-L8-64-64LQFP two chip system

Links marked NC are not required by the system topology. The I/O pins that overlap these xCONNECT links can be used for other purposes.

The constraints are:

1. The master which boots from SPI cannot use X0LA in 5 wire mode (because some pins are the SPI I/O pins).

2. All slave devices are connected in the master-ward direction using X0LB.

The XS1-LnA-128 devices are multi-tile modules containing two xCORE tiles interconnected in-package by four dedicated xCONNECT links that are not pinned out on the XS1-LnA-64 device family. Within the tile, the second tile is always booted through the first tile. Therefore to boot an XS1-LnA-128 device as a slave over xCONNECT links, link X0LB must be used. Any free outgoing link can then be used to boot further downstream devices.

6 Layout Guidelines

xCONNECT links are a transition-based protocol. As such, it is important that the transitions are delivered intact and in-order. As a general rule, you should treat a bundle of traces of an XMOS link as a clock signal; that is, amongst others:

- Separate the bundle from other PCB signals that would be disturbed by crosstalk from the XMOS-link
- Terminate each wire in the bundle to prevent reflections if the traces are routed over more than a short distance
- Do not route the signals close to noisy items on the PCB (such as switch-mode power supplies and clocks).
- If the traces are going over long distances, use low voltage differential signalling transceivers (LVDS) at each of the links to make these immune to common-mode interference and to improve the achievable symbol rate.
- Be aware that if the link driver has to drive a large capacitance (for example a long PCB trace), then that will increase variability in rise and fall times, requiring the link speed to be set slower.

When xCONNECT links are enabled, the wires should be logic low. Weak internal pull downs are active on the xCONNECT link pins before they are enabled. These pull downs cannot be relied upon to pull down long traces with high capacitance. Circuit designers should wire up external pull down resistors on such tracks.

7 Deployment Scenarios

The following xCONNECT link examples all operate error free with an inter symbol delay of 7.5ns.

- **2w link with 150mm FPC Flexible Ribbon Cable**

  Serial (2w) link utilizing 4 signal (2 per link direction) and 2 ground wires, with single ended drivers (for example 74AUP2G17) located at driving (TX) pins.

- **2w link with 150mm FPC Flexible Ribbon Cable and LVDS Transceivers**

  Serial (2w) link utilizing 8 signal (2 differential pairs per link direction) and 6 ground wires, with LVDS transceivers (for example DS90LV049) located at each end of each link wire.

- **2w link with 1000mm RJ45 double shielded cables and LVDS Transceivers**

Serial (2w) link utilizing 8 signal (2 differential pairs per link direction) and 2 ground wires, with LVDS transceivers (for example DS90LV049) located at each end of each link wire.

- **5w and 2w link with up to 100mm of PCB Track**

  Link with 33R series terminating resistors close to the TX sides of each wire, using no driver chips.

8 EMI

The EMI caused by the links, and the susceptibility to EMI interference are no different from any other electrical trace.

For emissions, the highest frequency signal to be expected is a single square wave with a period of twice the inter-symbol delay. For example, a five-wire link with an inter-symbol delay of 7.5 ns, may produce a 66.67 MHz square wave on one of the 5 traces.

Both EMI emissions and susceptibility should be tested as normal.