XK-XMP-64 Hardware Manual

(VERSION 1.0)

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1 Introduction

The XK-XMP-64 is 64 core multiprocessor based on the XMOS XS1-G4 event-driven processor. It comprises 16 XS1-G4, 16 LEDs, JTAG interface (over USB), two Ethernet interfaces, and two IDC expansion slots. These are outlined in Figure 1. They comprise:

A XS1-G4 Device ($\times$16)

B Green User LED ($\times$16)

C PLL Lock LED ($\times$16)

D USB-2.0 programming interface

E Ethernet connector ($\times$2)

F Reset Button

G Power Switch

H Power connector (12V, centre positive)

I Extension IDC connector ($\times$2)

The numbers in the diagram are the node numbers for each core, and the nodes to which the IO devices (Ethernet, IDC connector) are connected. Each XS1-G4 node contains four cores. The Ethernet connectors are connected to nodes 1 and 3, and that the IDC connectors are connected to nodes 0 and 2.

The following sections in this document provide a detailed description of these components.

2 XS1-G4 [A]

Each XS1-G4 device contains four multithreaded XCore™ processing components with tightly integrated support for communication, I/O and timing. The links of the XS1-G4s are connected to form a hypercube. In addition, some I/Os are available for Ethernet, lighting a LED or general purpose I/O.

The cores within node *nodeNumber* are numbered as follows:

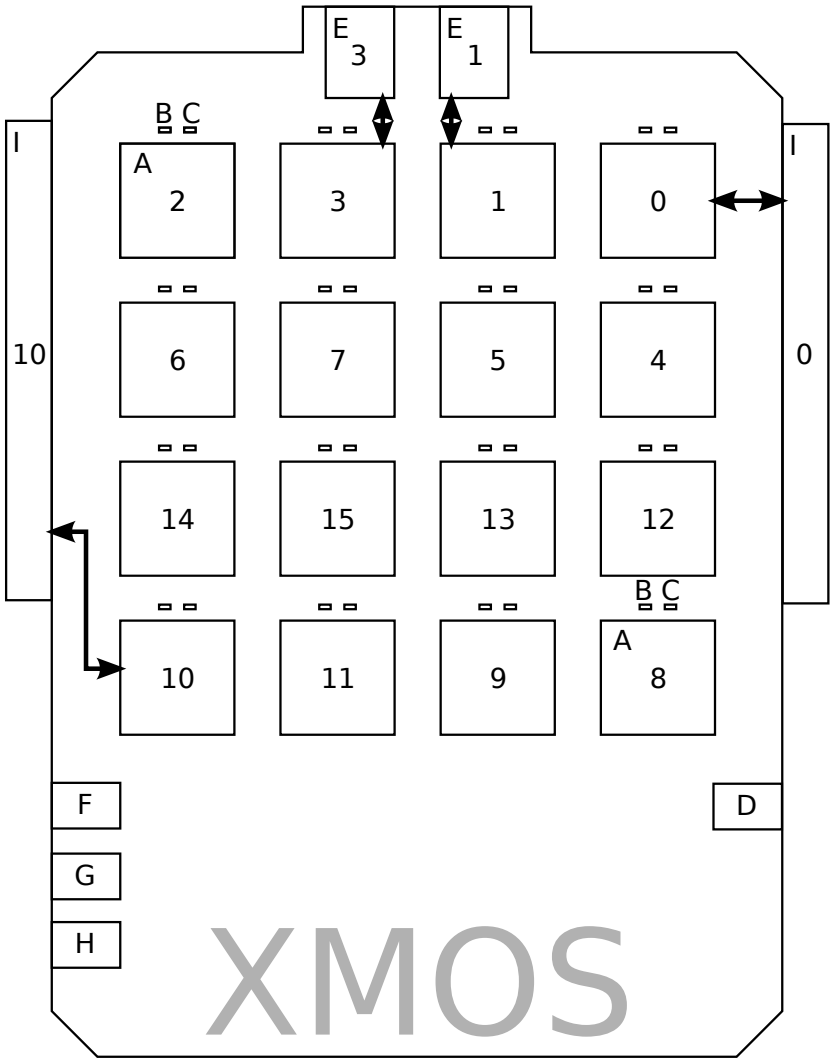

Figure 1 *Placement of components*

- $4 \times nodeNumber + 0$
- $4 \times nodeNumber + 1$
- $4 \times nodeNumber + 2$
- $4 \times nodeNumber + 3$

The nodes are connected in a hypercube network: there are four 400-Mbit links between node x and node y if and only if there is an integer $k \geq 0$ such that $x \oplus y = 2^k$

3 User-configurable LEDs [B]

These leds are green and can be lit by driving a "1" to port 1E on cores $4 \times k$: Core 0, Core 4, Core 8, ..., Core 56, and Core 60.

4 PLL Lock LEDs [C]

These leds are blue and should all be on during normal operation. The LED indicates that the core is clocked and not in RESET.

5 USB Connector [D]

The USB connector is used to load and debug code on all of the XS1-G4's processors. The USB connector provides JTAG control, system reset, and processor debug. The XK-XMP-64 has an embedded XTAG2 (the XMOS USB to JTAG key) with a serial number starting with "XMP".

6 Ethernet PHYs [E]

The left ethernet PHY is connected to Core 4 (Node 1, Core 0), the right ethernet PHY is connected to Core 12 (Node 3, Core 0).

7 Reset Button [F]

The XK-XMP-64 is reset on power up. If a reset is required this button can be pressed. When downloading code over USB the board is automatically reset.

8 Power Switch [G]

The power switch can be used to switch the power on or off.

9 Power Switch [H]

The board should be powered with a 12V 5A power supply (provided). The core should be positive. Internally, 1V (core), 1V8 (USB), 3V3 (I/O, links), and 5V (fans) are generated.

10 I/O Expansion Connectors [I]

Two connectors provide spare I/O to add additional hardware, for example an Audio codec. The left connector is connected to Cores 40 and 41 (Cores 2 and 3 on Node 10), the right connector is connected to Cores 2 and 3 (Cores 2 and 3 on Node 0)

11 XK-XMP-64 XN File

The XCore ports linked to the hardware features on the XK-XMP-64 are mapped to generic port identifiers as part of a platform specific XN file, which simplifies the process of porting a project between platforms.

11.1 I/O Port-to-Pin Mapping

The tables on the following pages provides a full description of the port-to-pin mappings. For each core it lists which I/Os are available.

Pin	Port				Core number				
	1b	4b	8b	16b	0	2	3	4	8
X*n*D12	P1E0				PORT_LED_0			PORT_LED_1	PORT_LED_2
X*n*D24	P1I0					$I_0$31	$I_0$3		
X*n*D25	P1J0					$I_0$32	$I_0$4		
X*n*D26		P4E0	P8C0	P16B0		$I_0$33	$I_0$5	PORT_ETH_RXD0_1	
X*n*D27		P4E1	P8C1	P16B1		$I_0$34	$I_0$6	PORT_ETH_RXD1_1	
X*n*D28		P4F0	P8C2	P16B2		$I_0$35	$I_0$7	PORT_ETH_TXD0_1	
X*n*D29		P4F1	P8C3	P16B3		$I_0$36	$I_0$8	PORT_ETH_TXD1_1	
X*n*D30		P4F2	P8C4	P16B4		$I_0$37	$I_0$9	PORT_ETH_TXD2_1	
X*n*D31		P4F3	P8C5	P16B5		$I_0$38	$I_0$10	PORT_ETH_TXD3_1	
X*n*D32		P4E2	P8C6	P16B6		$I_0$39	$I_0$11	PORT_ETH_RXD2_1	
X*n*D33		P4E3	P8C7	P16B7		$I_0$40	$I_0$12	PORT_ETH_RXD3_1	
X*n*D34	P1K0					$I_0$41	$I_0$13	PORT_ETH_TX_CLK_1	
X*n*D35	P1L0					$I_0$42	$I_0$14	PORT_ETH_TX_EN_1	
X*n*D36	P1M0		P8D0	P16B8		$I_0$45	$I_0$17	PORT_ETH_RX_CLK_1	
X*n*D37	P1N0		P8D1	P16B9		$I_0$46	$I_0$18	PORT_ETH_RX_DV_1	
X*n*D38	P1O0		P8D2	P16B10		$I_0$47	$I_0$19	PORT_ETH_RX_ER_1	
X*n*D39	P1P0		P8D3	P16B11		$I_0$48	$I_0$20	PORT_ETH_RX_MDC_1	
X*n*D40			P8D4	P16B12		$I_0$49	$I_0$21		
X*n*D41			P8D5	P16B13		$I_0$50	$I_0$22		
X*n*D42			P8D6	P16B14		$I_0$51	$I_0$23	PORT_ETH_NRST_1	
X*n*D43			P8D7	P16B15		$I_0$52	$I_0$24	PORT_ETH_MDIO_1	
X*n*D49		P32A0				$I_0$53	$I_0$25		
X*n*D50		P32A1				$I_0$54	$I_0$26		
X*n*D51		P32A2				$I_0$55	$I_0$27		
X*n*D52		P32A3				$I_0$56	$I_0$28		

Pin	Port				Core number			
	1b	4b	8b	16b	12	16	20	24
X*n*D12	P1E0				PORT_LED_3	PORT_LED_4	PORT_LED_5	PORT_LED_6
X*n*D26		P4E0	P8C0	P16B0	PORT_ETH_RXD0_3			
X*n*D27		P4E1	P8C1	P16B1	PORT_ETH_RXD1_3			
X*n*D28		P4F0	P8C2	P16B2	PORT_ETH_TXD0_3			
X*n*D29		P4F1	P8C3	P16B3	PORT_ETH_TXD1_3			
X*n*D30		P4F2	P8C4	P16B4	PORT_ETH_TXD2_3			
X*n*D31		P4F3	P8C5	P16B5	PORT_ETH_TXD3_3			
X*n*D32		P4E2	P8C6	P16B6	PORT_ETH_RXD2_3			
X*n*D33		P4E3	P8C7	P16B7	PORT_ETH_RXD3_3			
X*n*D34	P1K0				PORT_ETH_TX_CLK_3			
X*n*D35	P1L0				PORT_ETH_TX_EN_3			
X*n*D36	P1M0		P8D0	P16B8	PORT_ETH_RX_CLK_3			
X*n*D37	P1N0		P8D1	P16B9	PORT_ETH_RX_DV_3			
X*n*D38	P1O0		P8D2	P16B10	PORT_ETH_RX_ER_3			
X*n*D39	P1P0		P8D3	P16B11	PORT_ETH_RX_MDC_3			
X*n*D42			P8D6	P16B14	PORT_ETH_NRST_3			
X*n*D43			P8D7	P16B15	PORT_ETH_MDIO_3			

Pin	Port				Core number				
	1b	4b	8b	16b	28	32	36	40	41
X*n*D12	P1E0				PORT_LED_7	PORT_LED_8	PORT_LED_9	PORT_LED_10	
X*n*D24	P1I0							$I_{10}31$	$I_{10}3$
X*n*D25	P1J0							$I_{10}32$	$I_{10}4$
X*n*D26		P4E0	P8C0	P16B0				$I_{10}33$	$I_{10}5$
X*n*D27		P4E1	P8C1	P16B1				$I_{10}34$	$I_{10}6$
X*n*D28		P4F0	P8C2	P16B2				$I_{10}35$	$I_{10}7$
X*n*D29		P4F1	P8C3	P16B3				$I_{10}36$	$I_{10}8$
X*n*D30		P4F2	P8C4	P16B4				$I_{10}37$	$I_{10}9$
X*n*D31		P4F3	P8C5	P16B5				$I_{10}38$	$I_{10}10$
X*n*D32		P4E2	P8C6	P16B6				$I_{10}39$	$I_{10}11$
X*n*D33		P4E3	P8C7	P16B7				$I_{10}40$	$I_{10}12$
X*n*D34	P1K0							$I_{10}41$	$I_{10}13$
X*n*D35	P1L0							$I_{10}42$	$I_{10}14$
X*n*D36	P1M0		P8D0	P16B8				$I_{10}45$	$I_{10}17$
X*n*D37	P1N0		P8D1	P16B9				$I_{10}46$	$I_{10}18$
X*n*D38	P1O0		P8D2	P16B10				$I_{10}47$	$I_{10}19$
X*n*D39	P1P0		P8D3	P16B11				$I_{10}48$	$I_{10}20$
X*n*D40			P8D4	P16B12				$I_{10}49$	$I_{10}21$
X*n*D41			P8D5	P16B13				$I_{10}50$	$I_{10}22$
X*n*D42			P8D6	P16B14				$I_{10}51$	$I_{10}23$
X*n*D43			P8D7	P16B15				$I_{10}52$	$I_{10}24$
X*n*D49		P32A0						$I_{10}53$	$I_{10}25$
X*n*D50		P32A1						$I_{10}54$	$I_{10}26$
X*n*D51		P32A2						$I_{10}55$	$I_{10}27$
X*n*D52		P32A3						$I_{10}56$	$I_{10}28$

Pin	Port				Core number				
	1b	4b	8b	16b	44	48	52	56	60
X*n*D12	P1E0				PORT_LED_11	PORT_LED_12	PORT_LED_13	PORT_LED_14	PORT_LED_15

12 Related Documents

The following documents provide more information on designing with the XK-XMP-64:

- *XK-XMP-64 Tutorial*: provides an introduction to programming software on the XK-XMP-64 using the XC language.
- *The XMOS XS1 Architecture*: provides an overview of the XS1 instruction set architecture.
- *XK-XMP-64 Performance Measurements*: documents a number of performance measurements.

The most up-to-date information on the XK-XMP-64, including board schematics and product datasheets, is available from:

- `http://www.xmos.com/xmp64`

13 Document History

Date	Release	Comment
2010/02/22	1.0	First release.