MultiChannel Audio Slice Hardware Manual

Document Number: XM005709A

Publication Date: 2014/8/21

XMOS

Table of Contents

1 Overview 3

2 Main Board 5
- 2.1 Master Audio Clock . . . 6
  - 2.1.1 Fixed Mode . . . 6
  - 2.1.2 Recovered Mode . . . 6
- 2.2 Analogue Audio Out . . . 6
  - 2.2.1 PCM . . . 6
  - 2.2.2 TDM . . . 7
  - 2.2.3 DSD . . . 8
- 2.3 Analogue Audio In . . . 9
  - 2.3.1 PCM . . . 9
  - 2.3.2 TDM . . . 10
- 2.4 Digital Audio Loopback Testing . . . 11
- 2.5 MIDI . . . 12
  - 2.5.1 MIDI Receive . . . 12
  - 2.5.2 MIDI Transmit . . . 12
- 2.6 Digital Audio Out . . . 12
  - 2.6.1 Coaxial . . . 12
  - 2.6.2 Optical . . . 12
- 2.7 Buttons . . . 12
- 2.8 LED Array . . . 12
- 2.9 Power Supply Switching . . . 13

3 Support Board 14
- 3.1 Digital Audio In . . . 15
  - 3.1.1 Coaxial . . . 15
  - 3.1.2 Optical . . . 15
- 3.2 Button . . . 15
- 3.3 On Chip ADC . . . 15

4 Port Maps 16
- 4.1 Main Board Portmap PCM Mode . . . 16
- 4.2 Main Board Portmap DSD Mode . . . 17
- 4.3 Support Board Portmap . . . 17

5 Schematics 18

6 Errata 27

1 Overview

The XMOS MultiChannel Audio system is a hardware reference platform used to develop 8i/8o applications using the xCORE sliceKIT development platform.

The systems consists of two sliceCARDS, designed to interface with either a U16 or A16 sliceKIT Core Board. The main board is a double slot sliceCARD, and contains the analogue audio, MIDI, digital audio output and user I/O circuits, a support board contains the digital audio input and further user I/O.

Some key features of the system are listed below:

- 8 channel audio DAC, 24b up to 192kHz PCM, TDM DSD64 and DSD128
- 8 channel audio ADC, 24b up to 216kHz PCM and TDM
- Software selectable recovered or fixed local audio master clock PLL
- S/PDIF coaxial input and output
- S/PDIF or ADAT input and output
- Standard MIDI input and output interfaces
- User input buttons, and output 4x4 LED array
- Audio power supply enable for low power standby operation

A diagram of the system, connected to the U16 sliceKIT Core Board as an example, can be seen below:

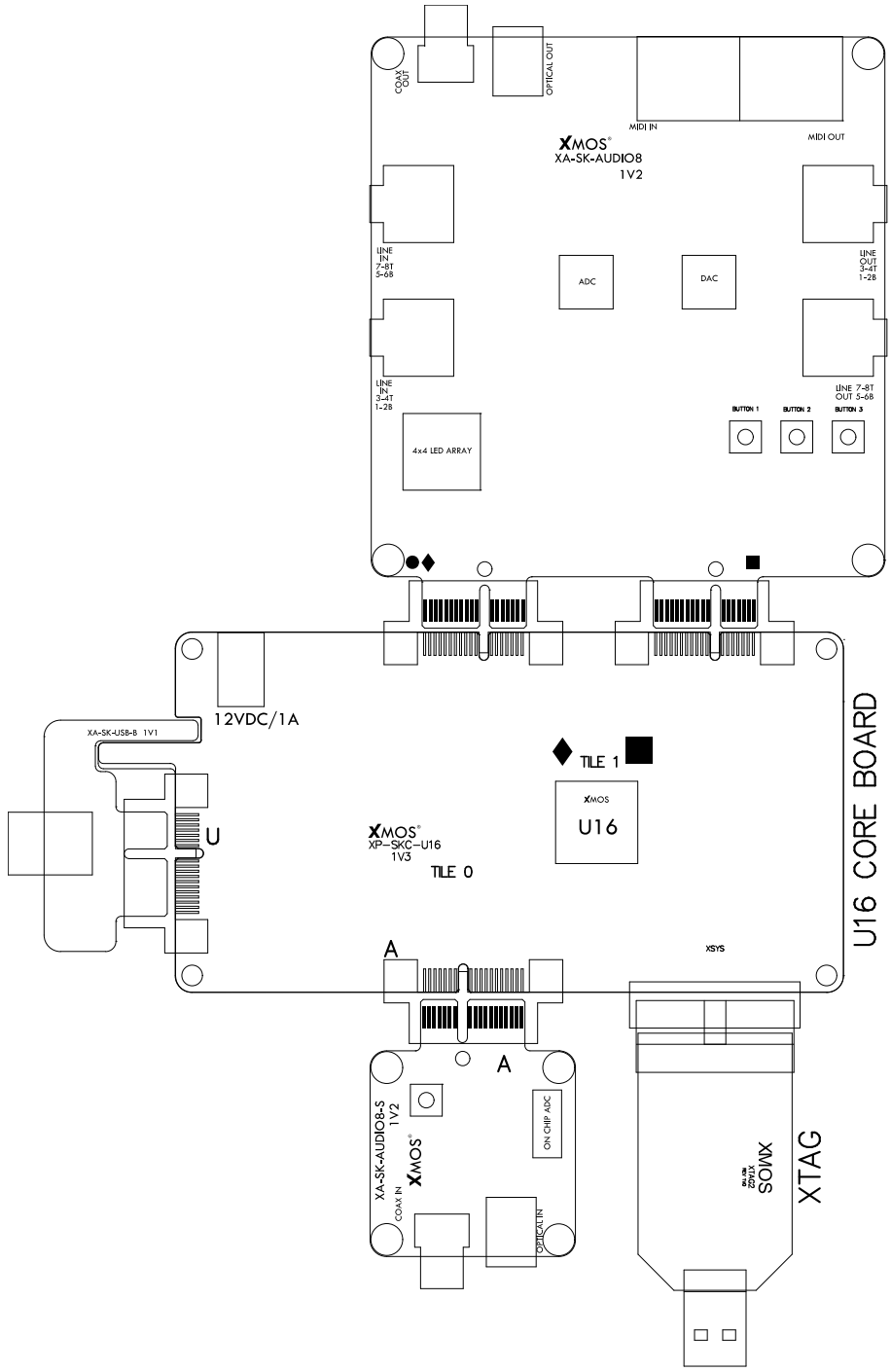

Figure 1: System Layout Example

2 Main Board

IN THIS CHAPTER

- Master Audio Clock
- Analogue Audio Out
- Analogue Audio In
- Digital Audio Loopback Testing
- MIDI
- Digital Audio Out
- Buttons
- LED Array
- Power Supply Switching

The main board (XA-SK-AUDIO8) contains the analogue audio, audio DAC, audio ADC, master clock PLL, digital audio output and user I/O circuitry.

This information in this section applies to revisions 1V1 and 1V2 of the XA-SK-AUDIO8 main board.

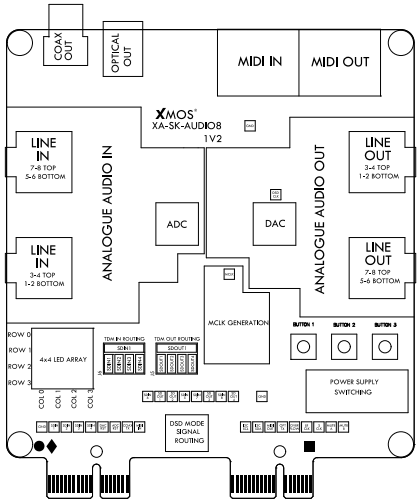

Figure 2: Main Board Layout

The diagram above details the layout and main sections of the main board.

2.1 Master Audio Clock

2.1.1 Fixed Mode

For systems that require a fixed local master clock, e.g. Isochronous USB audio, the output of a pre-programmed PLL device is used. This master clock option is selected by bringing the signal *PLL_SELECT* low (default).

The MCLK frequency is selected between 22.5792MHz and 24.576MHz by setting the *MCLK_FSEL* signal to the PLL device.

2.1.2 Recovered Mode

For systems that require a recovered master clock, e.g. AVB or S/PDIF, the output of a configurable PLL device is used. This master clock option is selected by bringing the signal *PLL_SELECT* high.

The MCLK frequency is set by configuring the PLL device using the I2C interface. The clock output can be recovered from the input clock source by providing a synchronisation signal on *PLL_SYNC*.

The I2C read address of the PLL is configured to be 0x9D and the write address 0x9C.

2.2 Analogue Audio Out

The board uses a 24 bit, 192kHz 8 channel audio DAC (Cirrus Logic® CS4384), capable of PCM, TDM and DSD 128x, for decoding the digital audio signal.

The DAC is configured in control port mode, allowing it to be configured using an I2C serial communications interface.

The I2C read address of the DAC is configured to be 0x31 and the write address 0x30.

The required operation mode and parameters such as MCLK divide should be set via the control port before operation begins.

The DAC analogue output channels are single ended, and go through a passive low-pass filter circuit, connected to a 3.5mm TRS jack socket. The output full scale signal is differential 3.35V pk-pk, this equates to 2.37V RMS. The output is AC coupled.

The low-pass filter is configured to reject signals above the nominal sample frequency of the ADC, with a cut-off frequency c. 130kHz.

2.2.1 PCM

In order to run the DAC in 8 channel PCM mode the jumpers should be set as follows:

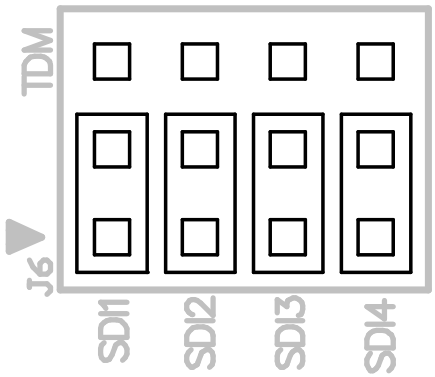

Figure 3: DAC PCM Jumper Settings

The eight channels of digital audio data should be clocked in to the DAC on the signals *SDIN[1:4]*.

When using PCM mode the signal *DSD_MODE* should be held low (default).

The DAC has three internal modes depending on the sampling rate used. These change the oversampling ratio used internally in the DAC. The table below show the required *MCLK* rates and ratios associated with the standard sample rates supported by the board:

Sample Rate (kHz)	MCLK (MHz)	MCLK Ratio	Speed-Mode	LRCLK (kHz)	BCLK (MHz)
44.1	22.5792	512x	Single-Speed	44.1	2.8224
48	24.576	512x	Single-Speed	48	3.072
88.2	22.5792	256x	Double-Speed	88.2	5.6448
96	24.576	256x	Double-Speed	96	6.144
176.4	22.5792	128x	Quad-Speed	176.4	11.2896
192	24.576	128x	Quad-Speed	192	12.288

Figure 4: DAC MCLK Frequencies for Standard Audio Sample Rates

The sample rate settings are the same as those or the ADC, allowing both ADC and DAC to operate at the same rates and ratios at the same time. The ADC and DAC can not run at different rates as they share the same I2S and master clocks.

2.2.2 TDM

In order to run the DAC in 8 channel TDM mode the jumpers should be set as follows:

The eight channels of digital audio data should be clocked in to the DAC on the signal *SDIN1*. It is possible to route any of the other SDIN signals to the DAC by

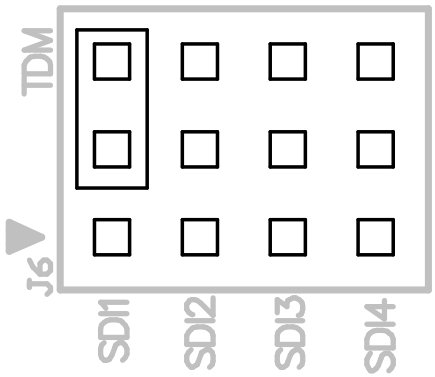

Figure 5: DAC TDM Jumper Settings

changing the position of the jumper in order to test systems with more than 8 channels using TDM.

When using TDM mode the signal *DSD_MODE* should be held low (default).

The TDM interface of the DAC will operate in single, double and quad speed modes. Data is clocked in on the first *BCLK* transition and is valid on the rising edge of *LRCLK*. The *LRCLK* is used to identify the start of a new frame, and should be equal to the sample rate.

Figure 6: DAC TDM MCLK Frequencies for Standard Audio Sample Rates

Sample Rate (kHz)	MCLK (MHz)	MCLK Div	Speed-Mode	LRCLK (kHz)	BCLK (MHz)
44.1	22.5792	2	Single-Speed	44.1	11.2896
48	24.576	2	Single-Speed	48	12.288
88.2	22.5792	2	Double-Speed	88.2	22.5792
96	24.576	2	Double-Speed	96	24.576

The sample rate settings are the same as those or the ADC, allowing both ADC and DAC to operate at the same rates and ratios at the same time. The ADC and DAC can not run at different rates as they share the same I2S and master clocks.

In TDM mode sample rates above 96kHz require a higher speed *MCLK* signal than can be provided by the fixed frequency PLL available on the board.

2.2.3 DSD

In order to run the DAC in 8 channel DSD mode the jumpers should be set as follows:

The eight channels of digital audio data should be clocked in to the DAC on the signals *SDIN[1:8]*.

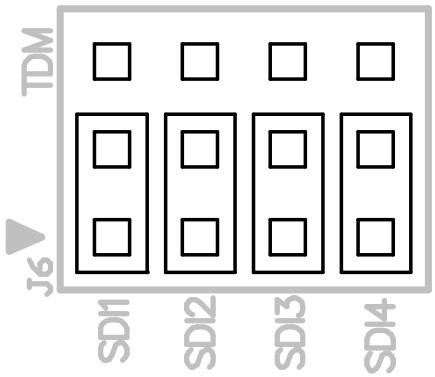

Figure 7: DAC TDM Jumper Settings

When using DSD mode the signal *DSD_MODE* should be held high, this will route the four ADC data lines (*SDIO[1:4]*) to the extra DAC input lines (*SDIN[5:8]*). The ADC can not be used while the DAC is in DSD mode and should be held in reset.

In DSD mode the *MCLK* should be set to 22.5792 MHz.

2.3 Analogue Audio In

The board uses a 24 bit, 192kHz 8 channel audio ADC (Cirrus Logic® CS5368) for encoding the analogue audio signal.

The ADC is configured in control port mode, allowing it to be configured using an I2C serial communications interface.

The I2C read address of the ADC is configured to be 0x99 and the write address 0x98.

The required operation mode and parameters such as MCLK divide should be set via the control port before operation begins.

The ADC analogue input channels are each fed from an active, single-ended to differential, low-pass filter circuit, connected to a 3.5mm TRS jack socket. The input full scale signal is 2V pk-pk, which will provide a 4V pk-pk differential signal to the ADC. The input is AC coupled to a filtered mid-supply voltage, which then feeds a unity gain low-pass filter, which drives the ADC input. The low-pass filter is configured to reject signals above the nominal sample frequency of the ADC.

2.3.1 PCM

In order to run the ADC in 8 channel PCM mode the jumpers should be set as follows:

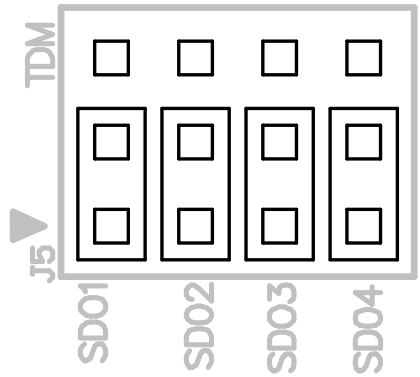

Figure 8: ADC PCM Jumper Settings

The eight channels of digital audio data should be clocked out of the ADC on the signals *SDIO[1:4]*.

When using the ADC the signal *DSD_MODE* should be held low (default).

The ADC has three internal modes depending on the sampling rate used. These change the oversampling ratio used internally in the ADC. The table below show the required *MCLK* rates and ratios associated with the standard sample rates supported by the board:

Figure 9: ADC MCLK Frequencies for Standard Audio Sample Rates

Sample Rate (kHz)	MCLK (MHz)	MCLK Div	Speed-Mode	LRCLK (kHz)	BCLK (MHz)
44.1	22.5792	2	Single-Speed	44.1	2.8224
48	24.576	2	Single-Speed	48	3.072
88.2	22.5792	2	Double-Speed	88.2	5.6448
96	24.576	2	Double-Speed	96	6.144
176.4	22.5792	2	Quad-Speed	176.4	11.2896
192	24.576	2	Quad-Speed	192	12.288

2.3.2 TDM

In order to run the ADC in 8 channel TDM mode the jumpers should be set as follows:

The eight channels of digital audio data should be clocked in to the ADC on the signal *SDIO1*. It is possible to route any of the other SDIO signals to the DAC by changing the position of the jumper in order to test systems with more than 8 channels using TDM.

When using ADC the signal *DSD_MODE* should be held low (default).

The TDM interface of the ADC will operate in single, double and quad speed modes. Data is clocked in on the first *BCLK* transition and is valid on the rising edge of

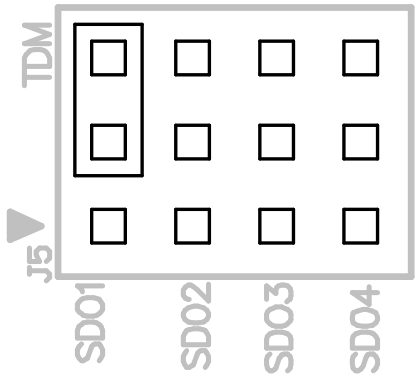

Figure 10: ADC TDM Jumper Settings

LRCLK. The *LRCLK* is used to identify the start of a new frame, and should be equal to the sample rate.

Figure 11: ADC TDM MCLK Frequencies for Standard Audio Sample Rates

Sample Rate (kHz)	MCLK (MHz)	MCLK Div	Speed-Mode	LRCLK (kHz)	BCLK (MHz)
44.1	22.5792	2	Single-Speed	44.1	11.2896
48	24.576	2	Single-Speed	48	12.288
88.2	22.5792	2	Double-Speed	88.2	22.5792
96	24.576	2	Double-Speed	96	24.576

In TDM mode sample rates above 96kHz require a higher speed *MCLK* signal than can be provided by the fixed frequency PLL available on the board.

2.4 Digital Audio Loopback Testing

It is possible to test the digital audio input and output by directly looping back the signals using patch wires between the headers J5 and J6. Refer to diagram below for a suggested test configuration.

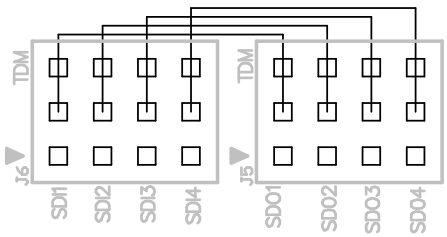

Figure 12: Loopback Jumper Cable Example

2.5 MIDI

2.5.1 MIDI Receive

Musical Instrument Digital Interface input is provided on the board via a standard DIN 5 180 degree connector (J9). The signal is isolated and buffered using an optical isolator and connected to the *MIDI_RX* signal, via a non inverting buffer.

A 220R pull up is placed on the receive signal from the isolator, this prevents glitches on start-up and when no MIDI devices are connected to the board.

2.5.2 MIDI Transmit

Musical Instrument Digital Interface output is provided on the board via a standard DIN 5 180 degree connector (J10). The signal is connected to the *MIDI_TX* signal via a non inverting buffer.

2.6 Digital Audio Out

2.6.1 Coaxial

An RCA phono connector (J12) is used to provide a digital audio output in IEC60958 consumer mode (S/PDIF) format. The S/PDIF signal is generated from the signal *COAXIAL_TX*. The data stream from the xCORE device is re-clocked using the external master clock to synchronize the data into the audio clock domain. This is achieved using a simple external D-type flip-flop.

2.6.2 Optical

A TOSLINK optical connector (J11), with an integrated LED and differential driver, is used to provide a digital audio output. It can be used to provide data using protocols including IEC60958 (S/PDIF) and ADAT Lightpipe. The data stream from the xCORE device is re-clocked using the external master clock to synchronize the data into the audio clock domain. This is achieved using a simple external D-type flip-flop.

2.7 Buttons

Three user input buttons are available on the main board. The button signal lines *BUTTON[1:3]* are pulled up with 10k resistors, depressing a button shorts the line to ground. The button signals are not physically debounced, this should be taken care of in the software.

2.8 LED Array

A 4x4 grid of LEDs is available as user output. The LEDs are arranged as a matrix, with four row (*LED_ROW_[0:3]*) and four column (*LED_COL_[0:3]*) inputs.

2.9 Power Supply Switching

The main board requires three power supply rails, 5.0V, 3.3V and 2.5V. The 2.5V supply is generated from the 5V supply to the board using an LDO linear regulator. The 5.0V and 3.3V supplies are taken from the sliceCARD interface. The 2.5V supply shares an enable signal *VA_EN* with a high-side switch device to allow the board to be powered down in a standby situation, this signal should be high to enable the power supplies to the main board.

3 Support Board

IN THIS CHAPTER

- Digital Audio In
- Button
- On Chip ADC

The support board (XA-SK-AUDIO8-S) contains the digital audio input and further user I/O circuitry.

This information in this section applies to revisions 1V1 and 1V2 of the XA-SK-AUDIO8-S support board.

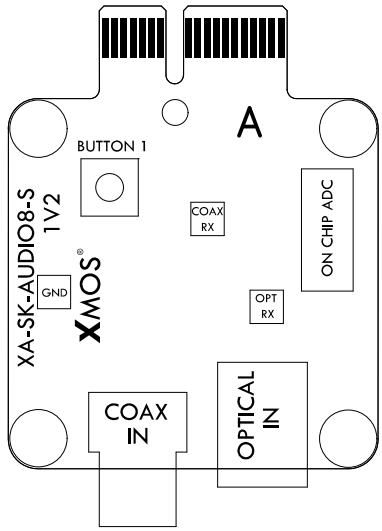

Figure 13: Support Board Layout

The diagram above details the layout and main sections of the support board.

3.1 Digital Audio In

3.1.1 Coaxial

An RCA phono connector (J4) is used to provide a digital audio input in IEC60958 consumer mode (S/PDIF) format. The S/PDIF signal is AC-coupled and fed into a differential line receiver, which in turn feeds the signal *COAX_RX*.

3.1.2 Optical

A TOSLINK optical connector (J3), with an integrated photodiode and receiver circuit, is used to provide a digital audio input. It can be used to provide data using protocols including IEC60958 (S/PDIF) and ADAT Lightpipe.

3.2 Button

An additional user input button is available on the support board. The button signal line *BUTTON1* is pulled up with a 10k resistor, depressing the button shorts the line to ground. The button signal is not physically debounced, this should be taken care of in the software.

3.3 On Chip ADC

The on chip ADC inputs of xCORE U16 and A16 devices, along with the 3.3V analogue power supply are made available to the user on the connector J1. The ADC inputs should never exceed the 3.3VA supply.

4 Port Maps

IN THIS CHAPTER

- Main Board Portmap PCM Mode
- Main Board Portmap DSD Mode
- Support Board Portmap

The port maps for U16 and A16 sliceKIT Core Boards, and the various modes of operation can be seen below.

4.1 Main Board Portmap PCM Mode

Signal	Signal Description	Dir	Slice Slot	Slice Pin	Alt Diamond	Port	Circle	Port2	Square	Port3
PLL_SYNC	Syncronisation signal for PLL	O	AD/C	B2	X1D0	P1A	X1D0	P1A		
SDIN1	Audio Data In 1 DAC [1:2]	O	AD/C	B4	X1D11	P1D	X1D11	P1D		
LED_C0	LED Column 0	O	AD/C	B6	X1D49	P32A0	X1D26	P4E0		
LED_C1	LED Column 1	O	AD/C	B7	X1D50	P32A1	X1D27	P4E1		
DAC_RST_N	DAC Reset (active low)	O	AD/C	B9	X1D26	P4E0	X1D28	P4F0		
SDIN4	Audio Data In 4 DAC [7:8]	O	AD/C	B10	X1D34	P1K	X1D34	P1K		
ADC_RST_N	ADC Reset (active low)	O	AD/C	B11	X1D27	P4E1	X1D29	P4F1		
SDIO1	Audio Data Out 1 ADC [1:2]	I	AD/C	B12	X1D36	P1M	X1D36	P1M		
SDIO2	Audio Data Out 2 ADC [3:4]	I	AD/C	B13	X1D37	P1N	X1D37	P1N		
SDIO3	Audio Data Out 3 ADC [5:6]	I	AD/C	B15	X1D24	P1I	X1D24	P1I		
SDIO4	Audio Data Out 4 ADC [7:8]	I	AD/C	B17	X1D38	P1O	X1D38	P1O		
MIDI_IN	MIDI Data Rx	I	AD/C	B18	X1D39	P1P	X1D39	P1P		
MCLK_XCORE	Audio MCLK Signal	I	AD/C	A3	X1D12	P1E	X1D12	P1E		
SDIN2	Audio Data In 2 DAC [3:4]	O	AD/C	A4	X1D23	P1H	X1D23	P1H		
LED_C2	LED Column 2	O	AD/C	A6	X1D51	P32A2	X1D32	P4E2		
LED_C3	LED Column 3	O	AD/C	A7	X1D52	P32A3	X1D33	P4E3		
SDIN3	Audio Data In 3 DAC [5:6]	O	AD/C	A8	X1D25	P1J	X1D25	P1J		
MCLK_FSEL	Audio MCLK Select	O	AD/C	A9	X1D32	P4E2	X1D30	P4F2		
DSD_MODE	DSD/PCM Mode Select	O	AD/C	A11	X1D33	P4E3	X1D31	P4F3		
LED_R2	LED Row 2	O	AD/C	A12	X1D65	P32A14	X1D42	P8D6		
LED_R3	LED Row 3	O	AD/C	A13	X1D66	P32A15	X1D43	P8D7		
COAX_TX	S/PDIF Coax Out	O	AD/C	A15	X1D35	P1L	X1D35	P1L		
LED_R0	LED Row 0	O	AD/C	A17	X1D63	P32A12	X1D40	P8D4		
LED_R1	LED Row 1	O	AD/C	A18	X1D64	P32A13	X1D41	P8D5		
I2C_SCL	I2C Clock	O	SQ	B6					X1D2	P4A0
MIDI_OUT	MIDI Data Tx	O	SQ	B9					X1D4	P4B0
OPT_TX	S/PDIF/ADAT Optical Out	O	SQ	B10					X1D10	P1C
BUTTON1	Button Input 1	I	SQ	B12					X1D14	P4C0
BUTTON2	Button Input 2	I	SQ	B13					X1D15	P4C1
SCLK	Audio Data Bit Clock	O	SQ	B15					X1D22	P1G
VA_EN	Audio Power Supply Enable	O	SQ	B17					X1D16	P4D0
PLL_SELECT	Select PLL (sync'd or standalone)	O	SQ	B18					X1D17	P4D1
I2C_SDA	I2C Data	IO	SQ	A8					X1D1	P1B
OVERFLOW	ADC Overflow Signal	I	SQ	A12					X1D20	P4C2
BUTTON3	Button Input 3	I	SQ	A13					X1D21	P4C3
LRCLK	Audio Data L/R Clock	O	SQ	A15					X1D13	P1F
MUTE_A	Mute Output A	O	SQ	A17					X1D18	P4D2
MUTE_B	Mute Output B	O	SQ	A18					X1D19	P4D3

Figure 14: Main Board Portmap PCM

4.2 Main Board Portmap DSD Mode

Signal	Signal Description	Dir	Slice Slot	Slice Pin	Alt Diamond	Port	Circle	Port2	Square	Port3
PLL_SYNC	Syncronisation signal for PLL	O	AD/C	B2	X1D0	P1A	X1D0	P1A		
SDIN1	Audio Data In 1 DAC [1]	O	AD/C	B4	X1D11	P1D	X1D11	P1D		
LED_C0	LED Column 0	O	AD/C	B6	X1D49	P32A0	X1D26	P4E0		
LED_C1	LED Column 1	O	AD/C	B7	X1D50	P32A1	X1D27	P4E1		
DAC_RST_N	DAC Reset (active low)	O	AD/C	B9	X1D26	P4E0	X1D28	P4F0		
SDIN4	Audio Data In 4 DAC [4]	O	AD/C	B10	X1D34	P1K	X1D34	P1K		
ADC_RST_N	ADC Reset (active low)	O	AD/C	B11	X1D27	P4E1	X1D29	P4F1		
SDIO1	Audio Data In 5 DAC [5]	O	AD/C	B12	X1D36	P1M	X1D36	P1M		
SDIO2	Audio Data In 6 DAC [6]	O	AD/C	B13	X1D37	P1N	X1D37	P1N		
SDIO3	Audio Data In 7 DAC [7]	O	AD/C	B15	X1D24	P1I	X1D24	P1I		
SDIO4	Audio Data In 8 DAC [8]	O	AD/C	B17	X1D38	P1O	X1D38	P1O		
MIDI_IN	MIDI Data Rx	I	AD/C	B18	X1D39	P1P	X1D39	P1P		
MCLK_XCORE	Audio MCLK Signal	I	AD/C	A3	X1D12	P1E	X1D12	P1E		
SDIN2	Audio Data In 2 DAC [2]	O	AD/C	A4	X1D23	P1H	X1D23	P1H		
LED_C2	LED Column 2	O	AD/C	A6	X1D51	P32A2	X1D32	P4E2		
LED_C3	LED Column 3	O	AD/C	A7	X1D52	P32A3	X1D33	P4E3		
SDIN3	Audio Data In 3 DAC [3]	O	AD/C	A8	X1D25	P1J	X1D25	P1J		
MCLK_FSEL	Audio MCLK Select	O	AD/C	A9	X1D32	P4E2	X1D30	P4F2		
DSD_MODE	DSD/PCM Mode Select	O	AD/C	A11	X1D33	P4E3	X1D31	P4F3		
LED_R2	LED Row 2	O	AD/C	A12	X1D65	P32A14	X1D42	P8D6		
LED_R3	LED Row 3	O	AD/C	A13	X1D66	P32A15	X1D43	P8D7		
COAX_TX	S/PDIF Coax Out	O	AD/C	A15	X1D35	P1L	X1D35	P1L		
LED_R0	LED Row 0	O	AD/C	A17	X1D63	P32A12	X1D40	P8D4		
LED_R1	LED Row 1	O	AD/C	A18	X1D64	P32A13	X1D41	P8D5		
I2C_SCL	I2C Clock	O	SQ	B6					X1D2	P4A0
MIDI_OUT	MIDI Data Tx	O	SQ	B9					X1D4	P4B0
OPT_TX	S/PDIF/ADAT Optical Out	O	SQ	B10					X1D10	P1C
BUTTON1	Button Input 1	I	SQ	B12					X1D14	P4C0
BUTTON2	Button Input 2	I	SQ	B13					X1D15	P4C1
SCLK	Audio Data Bit Clock	O	SQ	B15					X1D22	P1G
VA_EN	Audio Power Supply Enable	O	SQ	B17					X1D16	P4D0
PLL_SELECT	Select PLL (sync'd or standalone)	O	SQ	B18					X1D17	P4D1
I2C_SDA	I2C Data	IO	SQ	A8					X1D1	P1B
OVERFLOW	ADC Overflow Signal	I	SQ	A12					X1D20	P4C2
BUTTON3	Button Input 3	I	SQ	A13					X1D21	P4C3
LRCLK	Audio Data L/R Clock	O	SQ	A15					X1D13	P1F
MUTE_A	Mute Output A	O	SQ	A17					X1D18	P4D2
MUTE_B	Mute Output B	O	SQ	A18					X1D19	P4D3

Figure 15: Main Board Portmap DSD

4.3 Support Board Portmap

Signal	Signal Description	Dir	Slice Slot	Slice Pin	Mixed Signal	Port
COAX_RX	S/PDIF Coax In	I	MS	B2	X0D10	P1C
OPT_RX	S/PDIF/ADAT Optical In	I	MS	B4	X0D22	P1G
ADC0	xCORE ADC 0	I	MS	B6	ADC0	ADC0
ADC1	xCORE ADC 1	I	MS	B7	ADC1	ADC1
ADC2	xCORE ADC 2	I	MS	B10	ADC2	ADC2
ADC3	xCORE ADC 3	I	MS	B11	ADC3	ADC3
BUTTON1	Button Input 1	I	MS	B15	X0D1	P1B
ADC4	xCORE ADC 4	I	MS	A6	ADC4	ADC4
ADC5	xCORE ADC 5	I	MS	A7	ADC5	ADC5
ADC6	xCORE ADC 6	I	MS	A9	ADC6	ADC6
ADC7	xCORE ADC 7	I	MS	A17	ADC7	ADC7

Figure 16: Support Board Portmap

5 Schematics

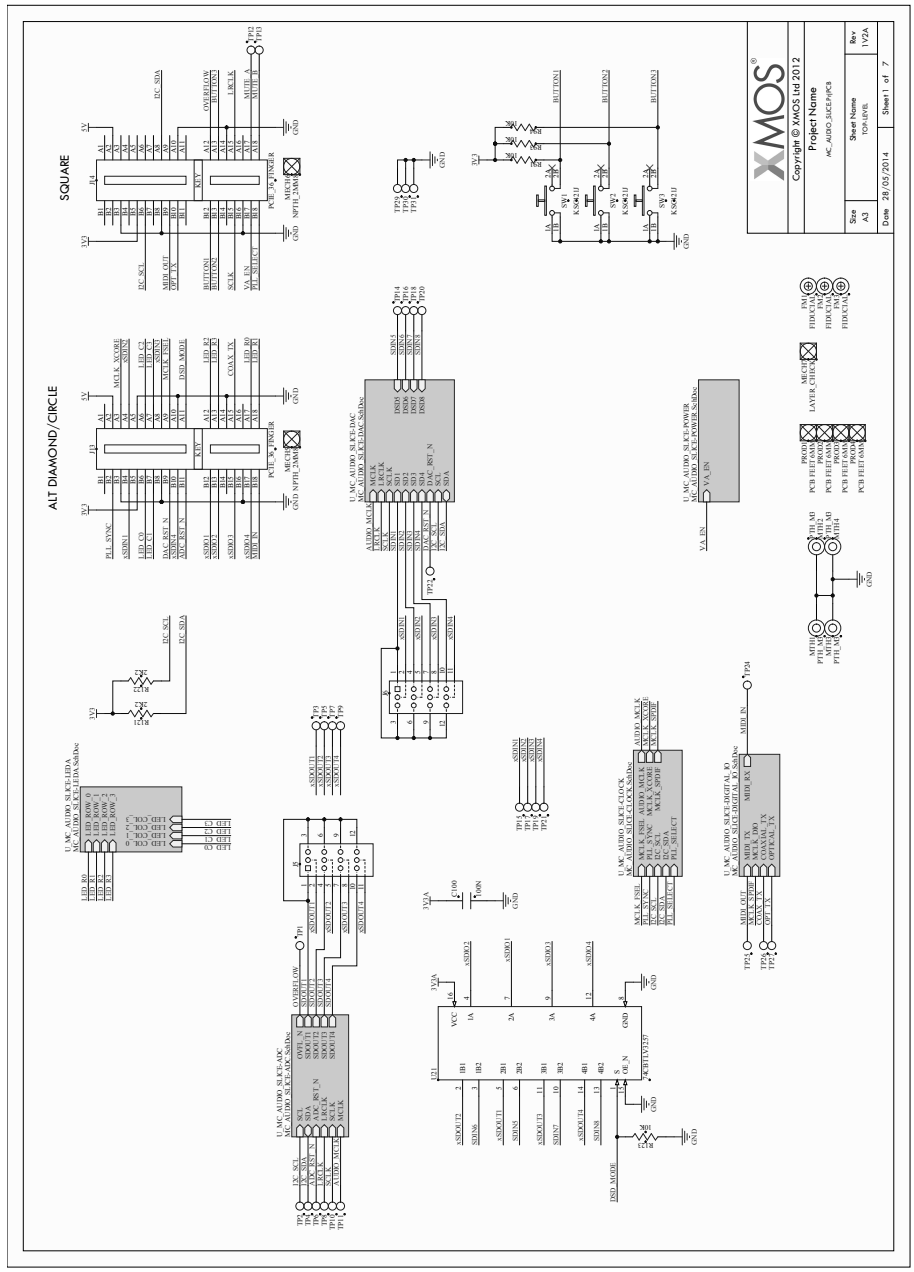

Figure 17: Top Level Schematic

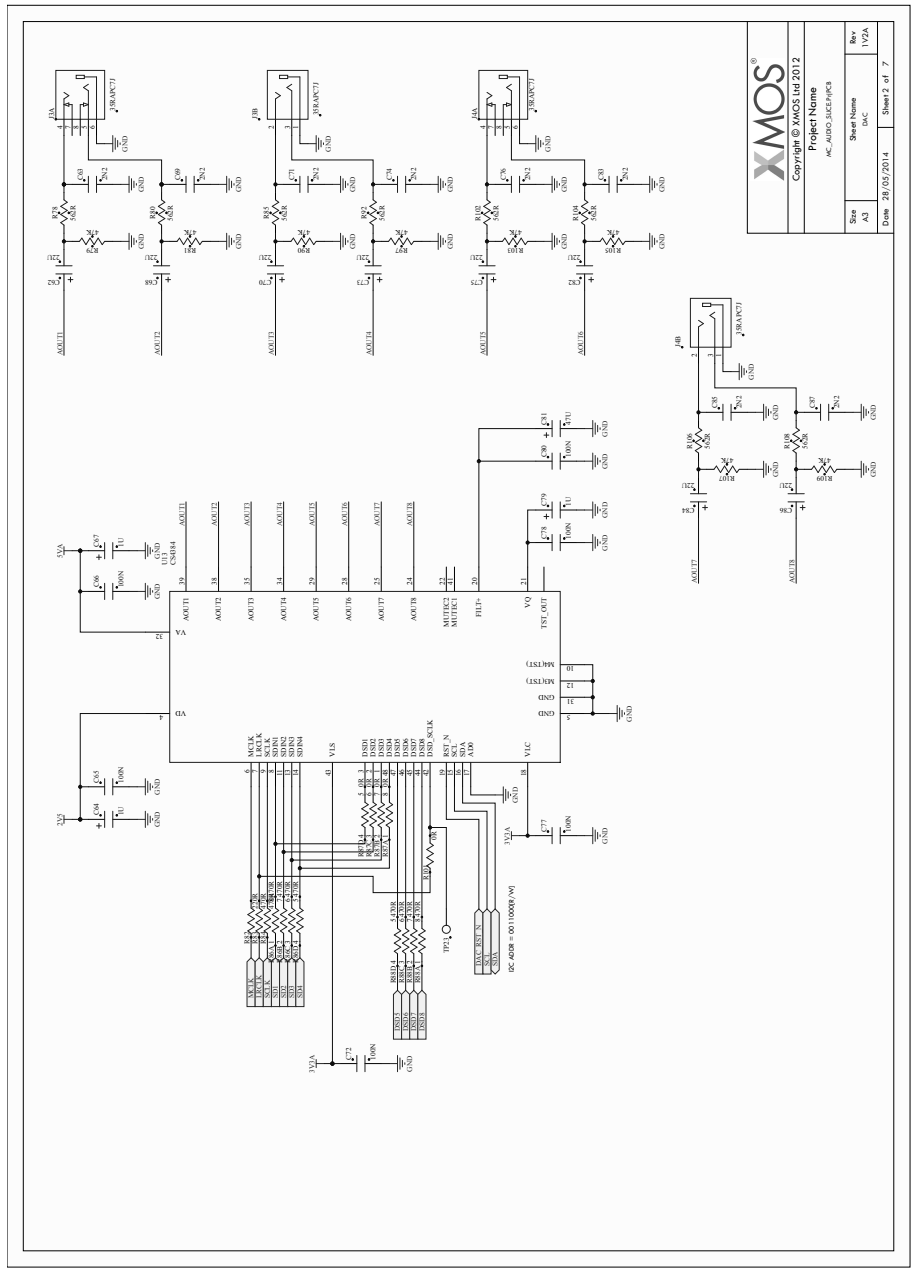

Figure 18: DAC Schematic

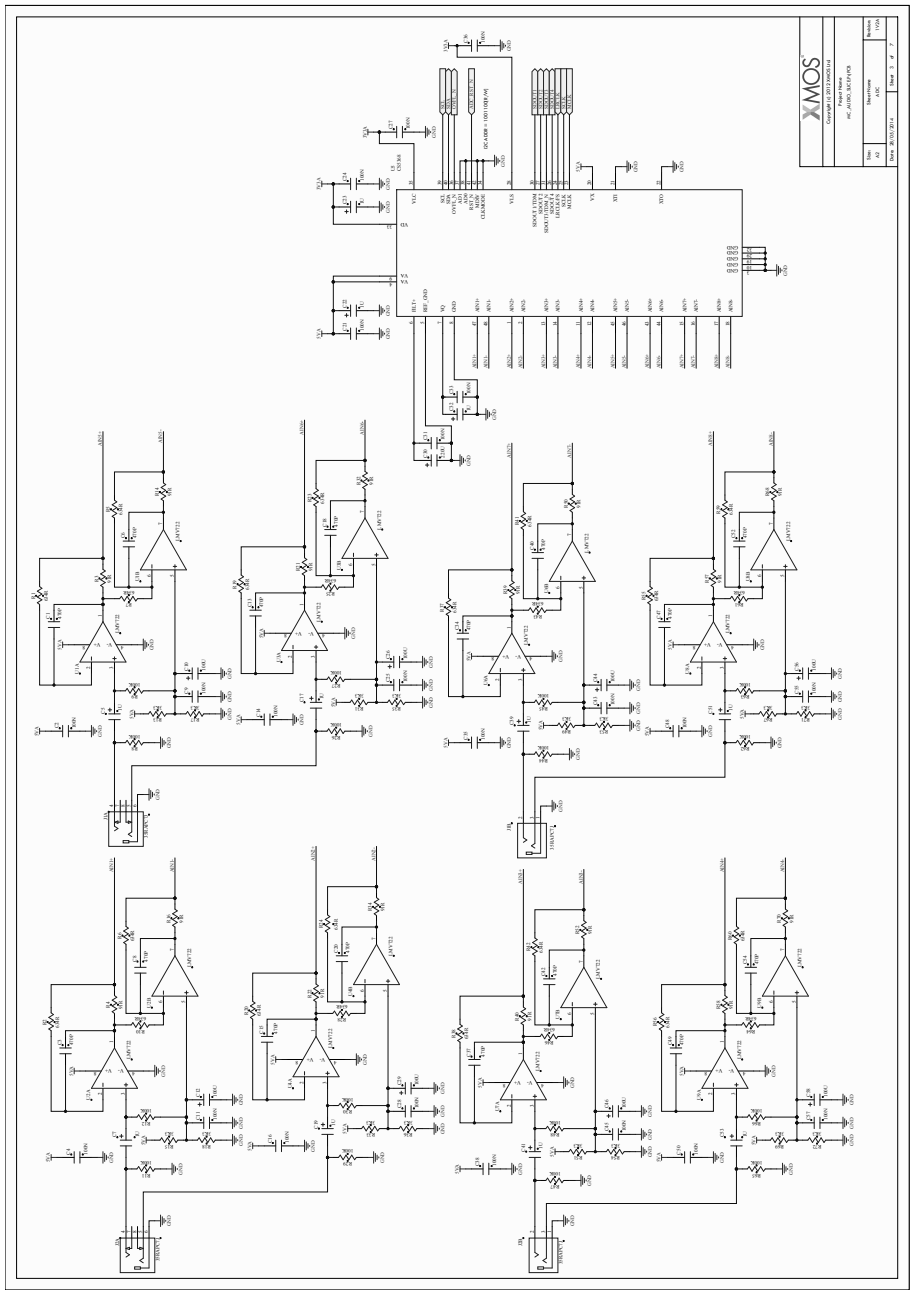

Figure 19: ADC Schematic

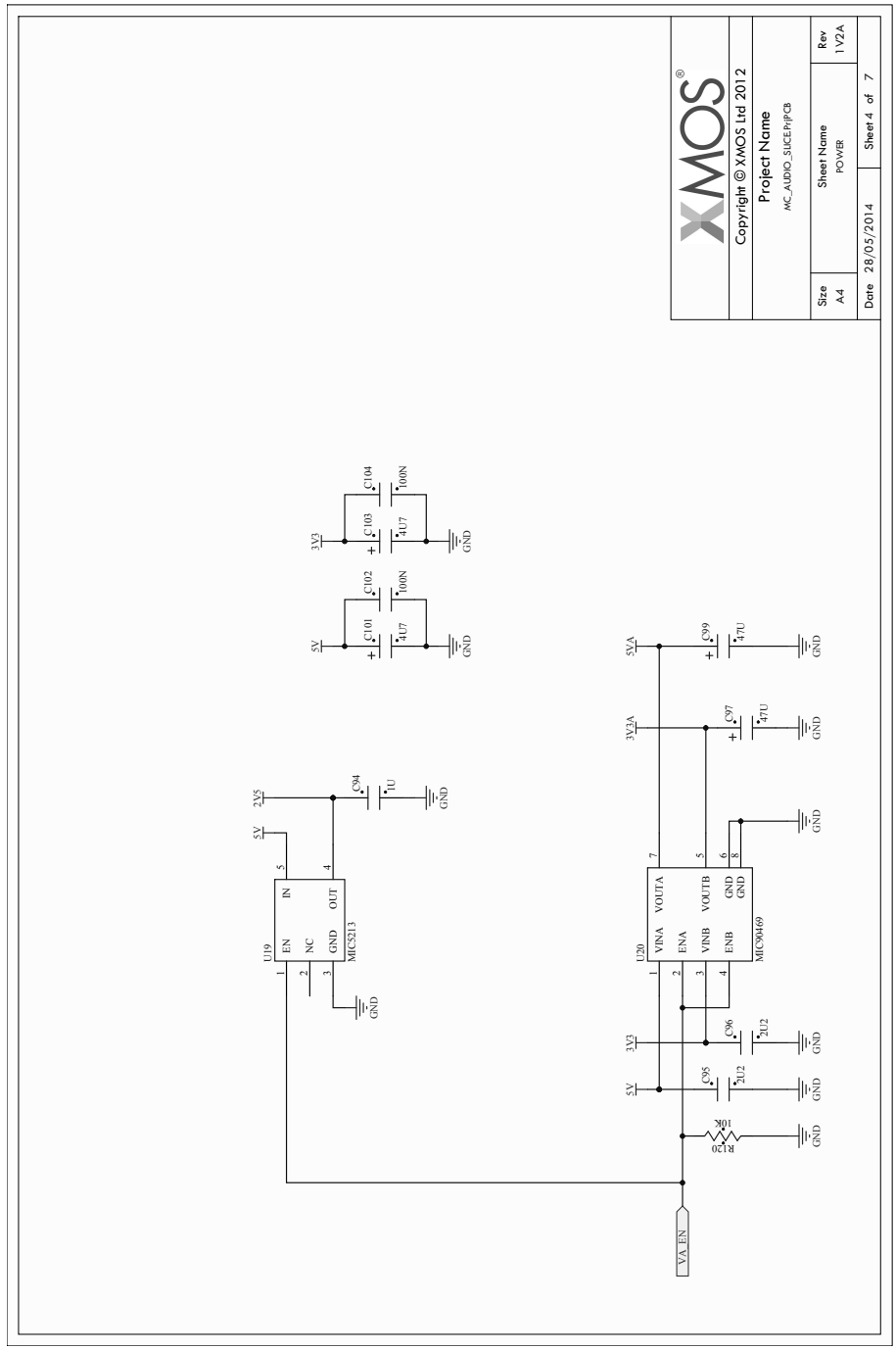

Figure 20: Power Schematic

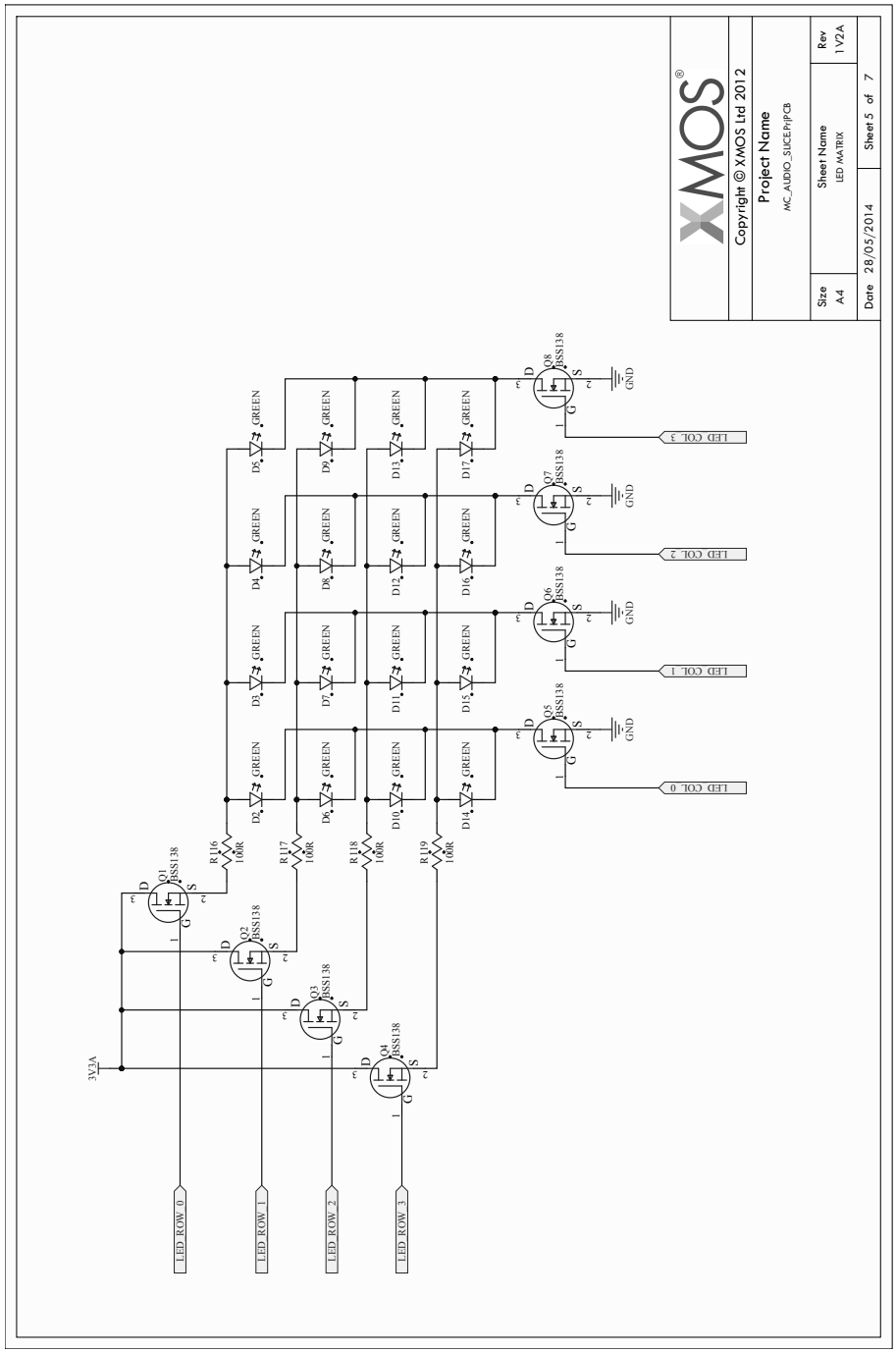

Figure 21: LED Array Schematic

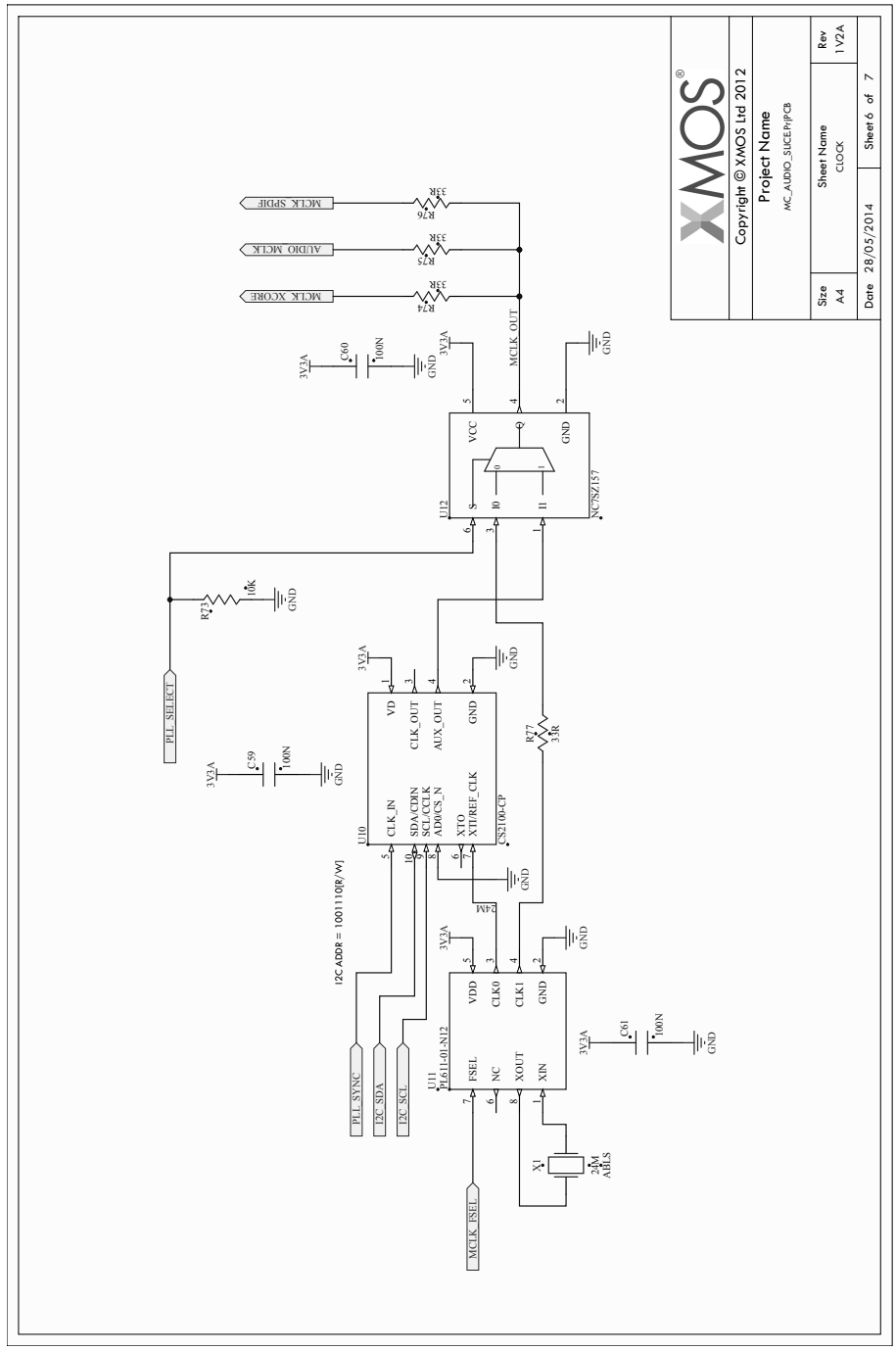

Figure 22: Clock Schematic

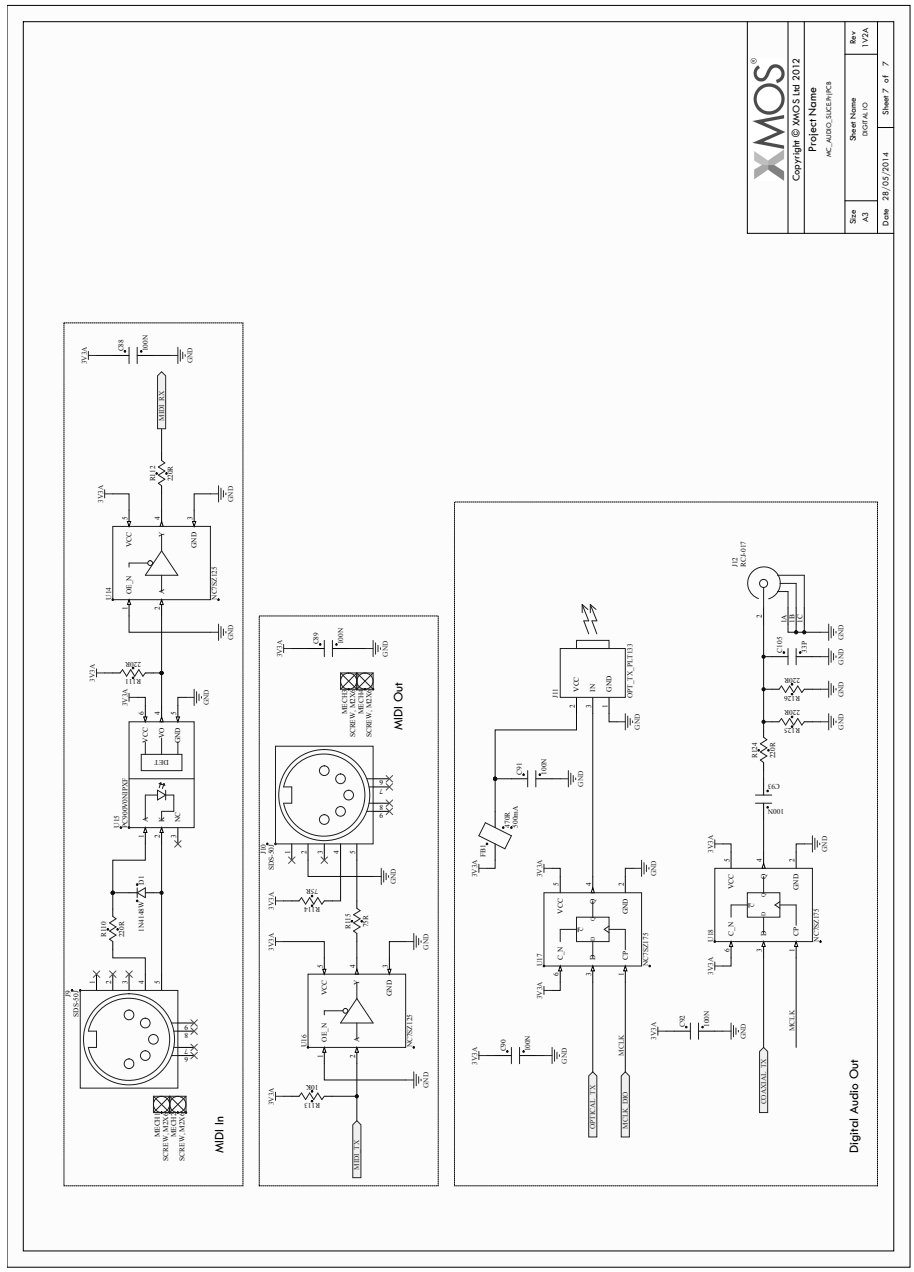

Figure 23: Digital Audio Schematic

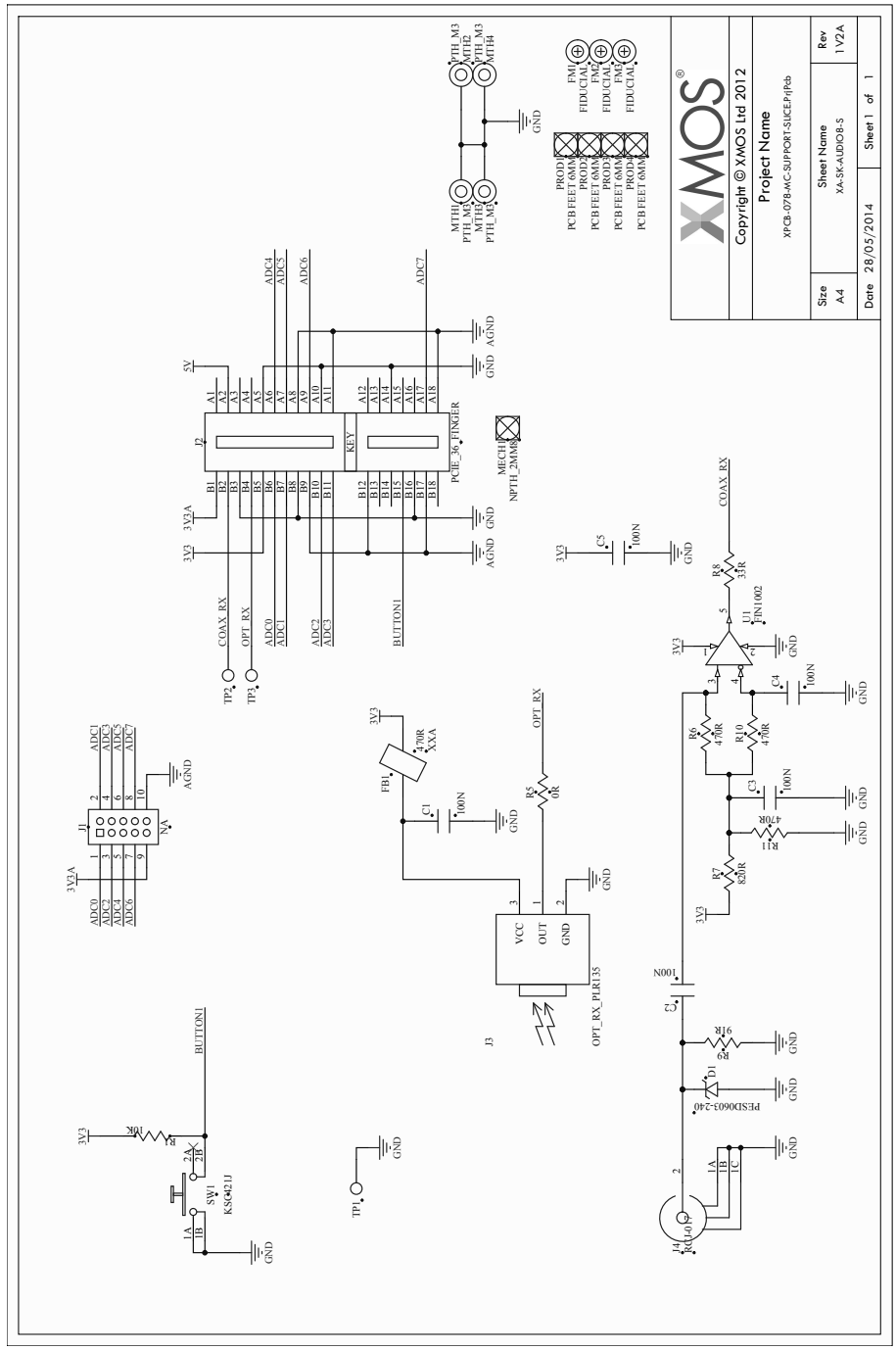

Figure 24: Support Board Schematic

6 Errata