VocalFusion XVF3620 Datasheet

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XMOS

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This datasheet provides advance information about the planned features, architecture, and operation of the VocalFusion® XVF3620, a high-performance voice processor, based on the XMOS XCORE.ai processor platform.

See also

The information in this datasheet should be read in conjunction with the *XU316-1024-QF60A* datasheet which contains electrical, design and integration data.

1 Key features

The VocalFusion® XVF3620 is a high-performance voice processor enabling voice control and communication with humans or robots in demanding acoustic environments. The combination of a complete voice pipeline with AI-denoising and a fast-adapting acoustic echo canceller (AEC) provides reliable capture even if it is noisy, reverberant, or involve a moving application.

The XVF3620 has the following key features:

1.1 Voice Processing

- AI-based denoising algorithm
- Full duplex Acoustic Echo Cancellation (AEC) with Residual Filtering (RES)
- Two PDM microphone interfaces
- Complete digital signal processing pipeline
- Programmable Automatic Gain Control (AGC)
- Flexible audio output routing and filtering options
- Reference audio via I^2S or USB

1.2 Device Interfaces

- High-speed speed USB 2.0 compliant device
- USB CDC and Endpoint 0 control interfaces
- I^2C interface for system control
- I^2S master or slave interface input & output of audio data

1.3 Firmware Management

- Boot from QSPI Flash
- Default firmware image for power-on operation
- Option to boot from a local host processor via SPI slave
- Device Firmware Update (DFU) via I^2C or USB

1.4 Package

- 7mm x 7mm 60pin QFN package

1.5 Power Consumption

- Typical power consumption: - UA mode: 315 mW - INT mode: 245 mW

2 Product overview

2.1 Scope

The XMOS VocalFusion® XVF3620 voice processor adds AI-based noise reduction to enable reliable audio capture with two microphones. The combination of a complete voice pipeline with AI and a fast-adapting acoustic echo canceller (AEC) enables voice control and communication with humans or robots in demanding acoustic environments - whether they are noisy, reverberant, or involve a moving application.

The processor is designed for seamless integration into consumer electronic products requiring voice interfaces for Automatic Speech Recognition (ASR), or communication. In addition to the class-leading voice processing, the XVF3620 processor implements specific features and interfaces required for use in integrated applications. The AI-based voice processing can be tuned for voice-recognition systems or human to human communication.

Two modes of operation are supported by the XVF3620:

- XVF3620-UA (USB Accessory) - Audio and control via a USB2.0 interface
- XVF3620-INT (INTegrated) - Audio via I^2S and control over I^2C interfaces

The functional block diagram of the XVF3620 is shown in the figures below:

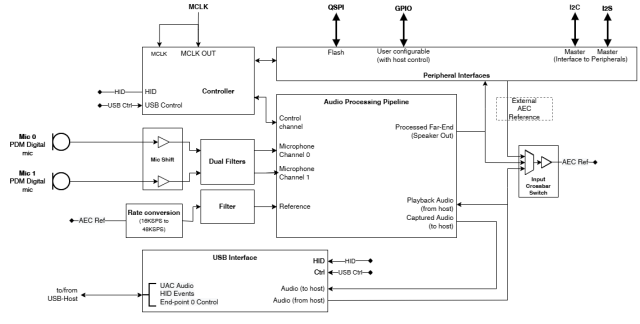

Fig. 1: Functional block diagram of XVF3620 in UA configuration

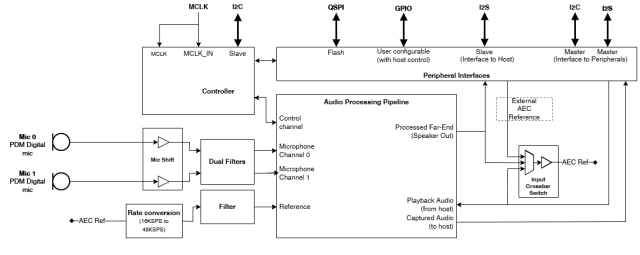

Fig. 2: Functional block diagram of XVF3620 in INT configuration

2.2 Audio Processing

The VocalFusion® XVF3620 voice processor converts and enhances audio captured using either a single microphone for cost sensitive applications or a pair of low-cost digital microphones for enhanced spatial filtering The processed audio streams are suitable for use in Automatic Speech Recognition or voice communications applications and benefit from a range of configurable audio processing techniques to allow customisation to the use case. The embedded audio processing provides the following features:

- Two microphone far-field operation.
- 48 kHz audio processing and I/O, sample rate voice DSP processing (16 kHz internal sample rate for voice capture & processing)
- Full duplex, fast adapting acoustic echo cancellation with enhanced residual supression accommodating highly reverberant environments.
- The reference audio for echo cancellation can be provided internally, via an I^2S interface (INT variant), via USB (UA variant).
- Advanced spatial filtering with modified generalised sidelobe cancelling algorithms to enhance audio from the desired direction and suppress diffuse background noise (2 microphones required).
- Adjustable AI-based denoiser.
- Adjustable gain with adjustable automatic gain control.

2.3 System firmware

The XVF3620 is available in two configurations:

- XVF3620-INT: using an I^2S/I^2C interface
- XVF3620-UA: using a USB interface

These are delivered as separate sets of firmware.

The VocalFusion® XVF3620 voice processor can be booted over SPI by a local host processor or from a separate, user-supplied, QSPI Flash memory. When operating with flash, the memory can be used for the following functions:

- A default firmware image for power-on operation.
- An upgrade image. Upgrades are provided via I^2C or USB providing a host-controlled upgrade process for over-the-air device management.

The XVF3620 can be upgraded and configured using the Device Firmware Upgrade (DFU) mechanism from the host processor. The DFU process is supported over either I^2C (INT variant) and USB (UA variant).

2.4 Example applications

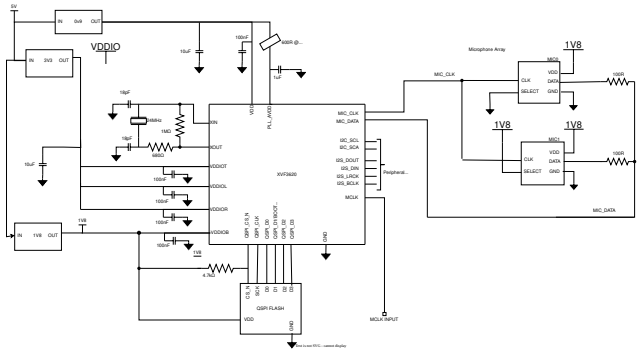

Fig. 3: Essential components of an XVF3620-INT application

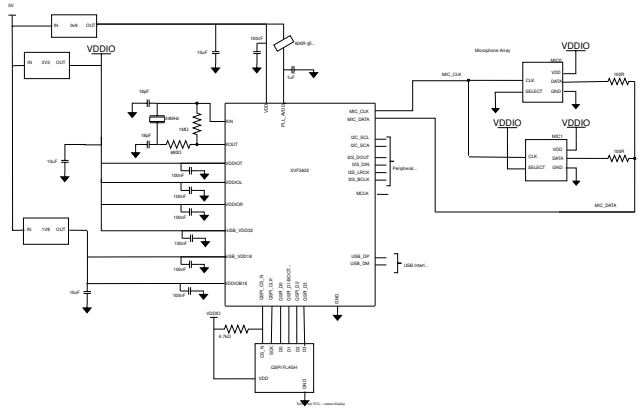

Fig. 4: Essential components of an XVF3620-UA application

3 Audio Processing

3.1 Signal processing pipeline

The XVF3620 audio processing pipeline takes inputs from a pair of MEMS Pulse Density Modulation (PDM) microphones and uses advanced signal processing to create audio streams suitable for use in Automatic Speech Recognition (ASR) and voice communication applications. The block diagram of this audio processing pipeline is shown in the figure below.

The pipeline enhances the captured audio stream using a set of complementary signal enhancement and noise reduction processes:

- **Microphone PDM to Pulse Code Modulation (PCM) conversion:** converts the PDM audio input from the microphones into PCM format allowing further processing.
- **Acoustic Echo Cancellation (AEC):** remove echoes that occur when the microphone picks up the sound played by the speaker again. This prevents the other party from hearing their own echo, which significantly improves voice quality. The models are continuously adapted to the acoustic environment to accommodate changes in the room created by events such as doors opening or closing and people moving in the

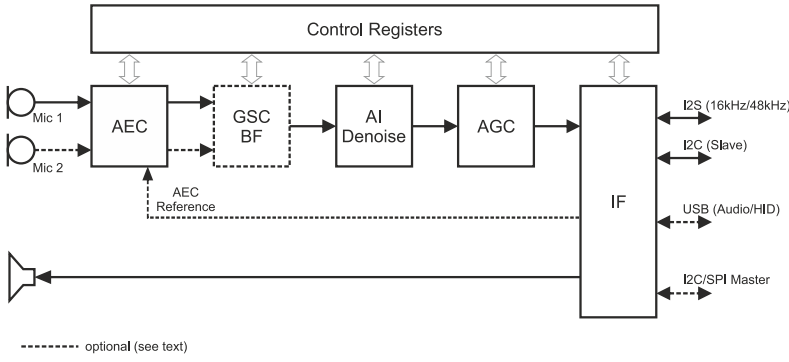

Fig. 5: The XVF3620 audio processing pipeline

room. The configurable loss-control and residual filtering allows fast adaptation times (<2 s) and excellent barge-in capabilities.

- **Beamformer (GSC):** A modified generalized sidelobe-canceler (beam-former) is used to selectively amplify signals from a specific direction and suppress interference and noise from other directions, giving a useful SNR advantage in demanding environments. The GSC requires two microphones.
- **AI denoising:** uses artificial intelligence to remove noise (e.g. hissing, humming, background noise) from audio. A trained model analyzes the data and specifically separates unwanted noise from the useful signal. Its adjustable SNR target significantly improves the quality for various applications.
- **Automatic Gain Control (AGC):** automatically adjusts the volume of an audio signal so that it is neither too quiet nor too loud. In contrast to MC/EQ, this works over a longer period of time and is also linked to speech detection

4 Pin diagram

4.1 Pin configuration

The pinout of the XVF3620, including all optional interfaces, is shown in the figure below.

Pins marked *RESERVED* are internally connected and should remain unconnected.

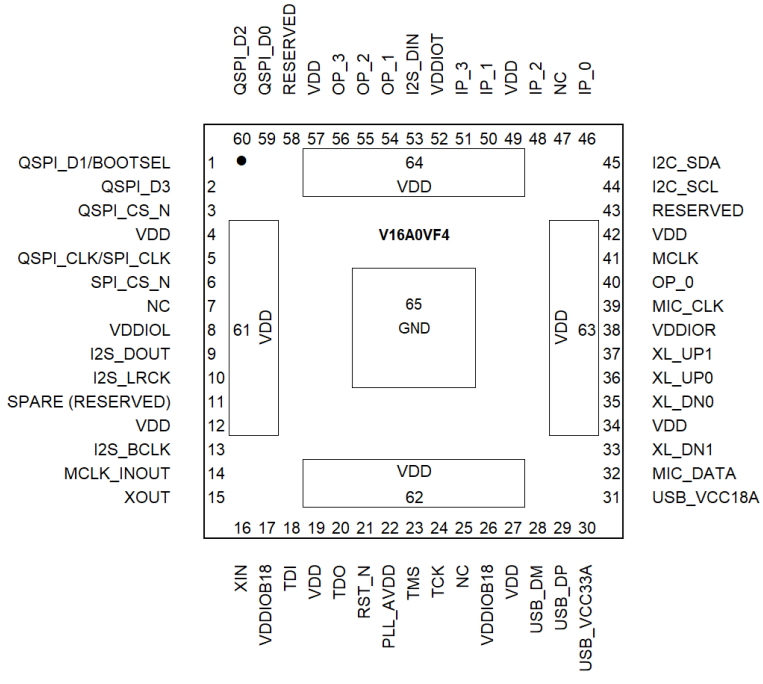

Fig. 6: `XVF3620-QF60A-C` pin configuration

Note

- VDDIOT, VDDIOL and VDDIOR should be connected a 1V8 supply
- VDDIO18 must be connected to a 1V8 supply and all VDD pins must be connected to a 0V9 supply.
- All package paddles (pins 61 to 65) must be connected.

4.2 Signal description

The table below lists the functions of all the pins shown in Fig. 6 above in the order they appear around the package.

> **Note**
>
> The function of some pins change depending on the firmware configuration loaded during boot (INT/UA).

Table 1: `XVF3620-QF60A-C` pin table

PIN	Signal Name	Description	Notes	Type
1	QSPI_D1/BOOTSEL	QSPI Data Line 1 and boot selection.	Pull high via a 4K7 ohm resistor to start in SPI Slave boot mode. Connect to D1 pin to boot from the QSPI flash memory.	I / O
2	QSPI_D3	QSPI Data Line 3		I / O
3	QSPI_CS_N	QSPI Boot Flash - Chip Select	Pull high externally to the device using a 4.7k ohm resistor	O
4	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR
5	QSPI_CLK/SPI_CLK	QSPI Clock		O
6	SPI_CS_N	Slave SPI boot / Peripheral SPI Master Chip Select	Pull high externally to the device using a 4.7k ohm resistor	I
7	NC	No Connection		
8	VDDIOL	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR
9	I2S_DOUT	I2S Data Out	Audio data out to host processor	O
10	I2S_LRCK	I2S Left/Right clock	48kHz or 16kHz clock derived as I2S_BLCK/64.	O (master), I (slave)
11	SPARE (RESERVED)			

continues on next page

Table 1 – continued from previous page

PIN	Signal Name	Description	Notes	Type
12	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR
13	I2S_BCLK	I2S bit synchronisation clock	48kHz (3.072MHz) sample rates	O (master), I (slave)
14	MCLK_INOUT	Master audio clock	Input in INT config; Output in USB Configs. Should be connected to Pin 41	I / O
15	XOUT	Crystal oscillator output	Pin should be left floating when using the CMOS clock input	O
16	XIN	Crystal oscillator input or CMOS clock input	Can be used as a clock input	I
17	VDDIOB18	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR
18	TDI	JTAG test data input	This pin has a weak internal pull-up	I
19	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR
20	TDO	JTAG test data output		O
21	RST_N	Device reset	Active low. Schmitt trigger input and an internal weak pull up	I
22	PLL_AVDD	Analogue power supply for core and application PLL.	Use a filtered version of the core supply, as per the XU316-1024 datasheet.	PWR
23	TMS	JTAG test mode select	This pin has a weak internal pull-up.	I
24	TCK	JTAG test clock input	Active low. Schmitt trigger input and an internal weak pull up	I
25	NC		Not connected. This pin should NOT be connected to any net	
26	VDDIOB18	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR
27	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR

continues on next page

Table 1 – continued from previous page

PIN	Signal Name	Description	Notes	Type
28	USB_DM		USB D- line. May be left floating if USB is not required	I / O
29	USB_DP		USB D+ line. May be left floating if USB is not required	I / O
30	USB_VCC33A		USB 3.3V power for the USB transceiver. May be left floating if USB is not required	PWR
31	USB_VCC18A		USB 1.8V power for the USB transceiver. May be left floating if USB is not required	PWR
32	MIC_DATA	PDM microphone input	DDR input - a pair of digital DDR microphones share this input	I
33	XL_DN1	XLINK	XSYS2 Debug port	I
34	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR
35	XL_DN0	XLINK	XSYS2 Debug port	I
36	XL_UP0	XLINK	XSYS2 Debug port	O
37	XL_UP1	XLINK	XSYS2 Debug port	O
38	VDDIOR	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR
39	MIC_CLK	Microphone clock output.	3.072MHz	O
40	OP_0	General purpose output		O
41	MCLK	Master audio clock		I
42	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR
43	RESERVED		Leave this pin unconnected	I
44	I2C_SCL	I2C serial clock line for receiving control command from I2C host		I / O
45	I2C_SDA	I2C serial data line		I / O
46	IP_0	General purpose input		I

continues on next page

Table 1 – continued from previous page

PIN	Signal Name	Description	Notes	Type
47	NC	No connection		
48	IP_2	General purpose input		I
49	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR
50	IP_1	General purpose input		I
51	IP_3	General purpose input		I
52	VDDIOT	I/O Power Supply (1v8)	All VDD pins must be connected.	PWR
53	I2S_DIN	Peripheral I2S interface - I2S data input		I
54	OP_1	General purpose output		O
55	OP_2	General purpose output		O
56	OP_3	General purpose output		O
57	VDD	Core power supply (0v9)	All VDD pins must be connected.	PWR
58	RESERVED	RESERVED	Leave this pin unconnected	
59	QSPI_D0	QSPI Data Line 0		I / O
60	QSPI_D2	QSPI Data Line 2		I / O
65	GND	Ground	All package paddles must be connected.	GND
61, 62, 63, 64	VDD	Core power supply (0v9)	All package paddles must be connected.	PWR

5 Device interfaces

5.1 PDM microphone inputs

Two standard PDM MEMS microphones should be connected to the MIC_DATA pin. The data input makes use of the left and right channel output capability of standard MEMS microphones and the microphone data is read on alternative edges of the MIC_CLK signal. The XVF3620 reads one microphone on the positive edge of the microphone clock and the other microphone on the negative edge of the clock.

The XVF3620 outputs a microphone clock at 3.072MHz on the MIC_CLK output, which must be fed directly to both microphones. This signal must be used to clock the microphone PDM output to avoid undefined artefacts in the processed audio stream. One microphone should be set to be left (output on rising edge of clock) and the other right (output on the falling edge of clock).

An example microphone circuit is shown in the figure below:

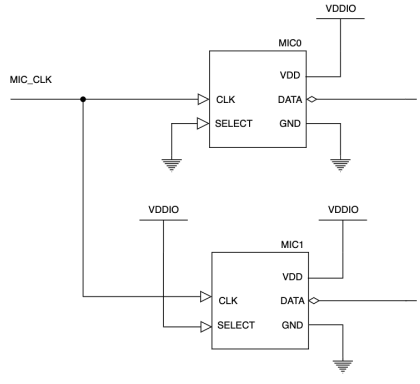

Fig. 7: PDM microphone schematic

The voice processor has been tested and characterised with microphones placed with a 71mm separation and connected to the product enclosure in such a way that the acoustic path to each microphone from outside the product is independent. The XVF3620 algorithms automatically adapt to alternative spacing, but differences in audio performance may occur and should be thoroughly characterised.

5.2 QSPI boot mode

When QSPI boot mode is enabled (default), the XVF3620 enables the six QSPI pins, see table below, and drives the QSPI clock as a QSPI Master. A READ command is issued with a 24-bit address 0x000000.

Table 2: QSPI signals

Signal	Description	Comment	Pin	I/O
QSPI_CS_N	QSPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	3	O
QSPI_CLK / SPI_CLK	QSPI Clock		5	O
QSPI_D0	QSPI Data Line 0		59	I/O
QSPI_D1 / BOOTSEL	QSPI Data Line 1	Tie high via 4.7k ohm resistor to start in SPI Slave boot mode. If connected to a QSPI D1 pin on a memory device the device will start in QSPI Master mode	1	I/O
QSPI_D2	QSPI Data Line 2		60	I/O
QSPI_D3	QSPI Data Line 3		2	I/O

For further information about the boot sequence refer to the *XU316-1024-QF60A* datasheet.

5.3 SPI interface

The SPI interface can be utilised in both Master and Slave configurations for peripheral control of components like DACs and ADCs (master), and SPI boot from host a host processor (slave).

5.3.1 Peripheral component control

Once the XVF3620 has successfully booted, the SPI interface can be used to configure peripheral components such as DACs, ADCs and keyword detection devices. In this mode the SPI interface operates as a master, and transfers data held in flash, or received from the host over the control interface.

For further information on this configuration consult the *XU316-1024-QF60A* datasheet.

5.3.2 SPI slave boot mode

To enable SPI boot from an external host processor, the QSPI_D1/BOOTSEL should be pulled to VDDIO on power-up. This activates the SPI interface, which operates as a slave to the host processor for the transfer of the boot image, which is clocked in with the least significant bit first in each transferred byte.

The SPI pins are shown below in the table below.

Table 3: SPI signals

Signal	Description	Comment	Pin	I/O
SPI_CLK	SPI Clock		5	I
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	6	I
SPI_MOSI	SPI Master Out Slave In		7	I
SPI_MISO	SPI Master In Slave Out	May be left floating if not required	47	O

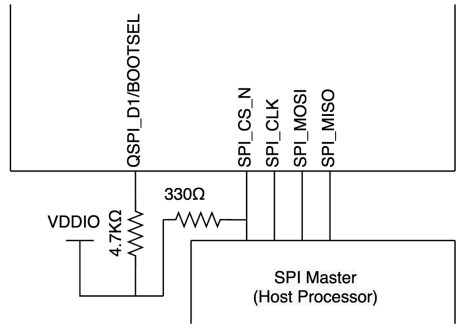

Fig. 8: XVF3620 SPI Slave boot configuration

5.4 Integrated USB interface

The USB interface is used to deliver processed voice audio to the host processor, stereo reference audio from the host and as a control interface. In this mode the USB Audio endpoint is used to generate an MCLK which is driven out of MCLK_INOUT pin.

The USB interface will use XMOS Vendor ID `0x20B1`. The USB Product ID presented depends on the mode:

- When in USB Audio Class 1.0 mode, the XVF3620 will present USB Product ID `0x4E01`.
- When in USB Audio Class 2.0 mode, the XVF3620 will present USB Product ID `0x4E02`.
- When in Device Firmware Update (DFU) mode, the XVF3620 will present USB Product ID `0x4E00`.

The table below shows the signals required to implement a USB interface using the XVF3620.

Table 4: USB connections

Name	Description	Pin
USB_DP	Connect to USB connector	29
USB_DM	Connect to USB connector	28
USB_VBUS_DET	Do not connect Self-powered operation is not supported by current device firmware	43
USB_VDD18	1.8V supply for USB-PHY - May be left floating if the USB interface is not used	31
USB_VDD33	3.3V supply to the USB-PHY May be left floating if the USB interface is not used	30

Note

The UA firmware only supports use in a bus powered configuration where VBUS is present. Self-powered configurations are not supported.

5.5 I²S audio interface

The I²S interface operates in different modes depending on the firmware configuration.

- XVF3620-INT operates as an I²S Slave outputting audio to the host processor and receiving the reference audio signal.
- XVF3620-UA implements an I²S Master outputting audio for the loudspeakers.

The flow of audio samples must be synchronised to a single set of I²S clocks, see table below:

Table 5: I²S signals

Signal	Description	Comment	Pin	I/O
MCLK	Master audio clock		14	I
I2S_BCLK	I²S bit synchronisation clock	Configurable for 16kHz (1.024MHz) and 48kHz (3.072MHz) sample rates	13	I
I2S_LRCK	I²S Left/Right clock	48kHz clock derived as I2S_BLCK/64	10	I
I2S_DIN	I²S Data In	Reference audio data from I²S device	53	I
I2S_DOUT	I²S Data Out	Audio data out	9	O

The I²S audio samples are transmitted serially with a one I2S_BCLK delay between the change of I2S_LRCK phase and the start (MSB) of the audio sample for that channel. This the standard alignment for I²S systems.

5.6 I²C control interface

The I²C Slave interface is used to control and configure the parameters on the XVF3620-INT.

The device I²C address is 0x2A, and the pin connections are shown below.

Table 6: I²C Slave Connections

Signal	Description	Comment	Pin	I/O
I2C_SCL	I²C serial clock line for receiving control command from I²C host		44	I/O
I2C_SDA	I²C serial data line for receiving control command from I²C host		45	I/O

Note

I²C commands received prior to I²S clocks being activated will not be processed and may result in undefined behaviour. Therefore, it is important to ensure that the I²S interface is activated before accessing the device over I²C.

For more information on control and configuration of the XVF3620 please refer to "sw_xvf3620 – Documentation" available on XVF3620 product page.

5.7 General purpose input/output

Four input and four output pins are provided to allow general-purpose I/O such as LEDs and button controls. Input pins can be individually read by the host using the control interface and configured to detect edge events. The output pins can be individually set.

The GPIO pins are shown in the table below.

Table 7: GPIO pin table

Name	Description	Pin	I/O
IP_0	General purpose input	46	I
IP_1	General purpose input	50	I
IP_2	General purpose input	48	I
IP_3	General purpose input	51	I
OP_0	General purpose output	40	O
OP_1	General purpose output	54	O
OP_2	General purpose output	55	O
OP_3	General purpose output	56	O

For more information on these inputs and outputs, please refer to the *XU316-1024-QF60A*.

6 Device operation

6.1 Power supplies

The XVF3620 has the following power supply pins:

Table 8: XVF3620 Power Pins

Name	Description	Pin
VDD	Digital core power supply. 0.9V (nominal)	4 12 19 27 34 42 49 57 61 64
V_DDIOL	Digital I/O power supply ** See Note A	8
V_DDIOR	Digital I/O power supply ** See Note A	38
V_DDIOT	Digital I/O power supply ** See Note A	52
VDD IOB18	Digital I/O power supply. 1.8V (nominal)	17 - 26
PLL_AVDD	PLL analogue power. This 0.9V (nominal) PLL supply should be separated from the other supplies at the same voltage by a low pass filter	22
USB_VDD18	Digital supply to the USB-PHY. 1.8V (nominal)	31
USB_VDD33	Analogue supply to the USB-PHY. 3.3V (nominal)	30
VSS	Device Ground	65 (Paddle)

See also

The *XU316-1024-QF60A* datasheet contain further information on power supplies and power on sequencing.

6.2 Clocks

The XVF3620 device has an on-chip oscillator. To use the oscillator a crystal, two capacitors, and damping and feedback resistors to the device as shown below.

Table 9: XVF3620 crystal oscillator

Signal	Description	Comment	Pin	I/O
XIN	Crystal oscillator input		16	I
XOUT	Crystal oscillator output		15	O

Alternatively, the XVF3620 can be provided with a 24MHz, 1V8 clock input on the XIN pin. The clock must be running when the chip comes out of reset.

Fig. 9: Crystal oscillator or clock input configurations

Table 10: XVF3620 clock signals

Signal	Description	Comment	Pin	I/O
XIN	Master clock (system)	24MHz 1V8 clock signal	16	I
XOUT	N/C	Leave floating if clock input on XIN	15	O

See also

For further information, and details on the calculation of R_f and R_d, please refer to the *XU316-1024-QF60A* datasheet.

6.3 Reset

The XVF3620 device has an on-chip Power-on-Reset (POR). This keeps the chip in reset whilst the supplies are coming up.

See *XU316-1024-QF60A* datasheet for further information.

Table 11: Reset Signal

Signal	Description	Comment	Pin	I/O
RST_N	Device reset	Active low	21	I

6.4 Boot modes

On start-up and after a reset event, the XVF3620 is booted either using an externally connected QSPI flash memory or by transferring a boot image to the device via SPI from a host processor.

6.4.1 QSPI master boot mode

If the QSPI_D1/BOOTSEL pin is connected to a QSPI_D1 pin on a flash device, the XVF3620 will boot from the local QSPI flash in QSPI Master mode. The active pins are shown below.

Table 12: QSPI Master peripheral interface pins

Name	Description	Pin	I/O
QSPI_CS_N	QSPI Chip Select. This pin should be pulled high externally to the device using a 4.7k ohm resistor	3	I/O
QSPI_D0	QSPI Data Line 0	59	I/O
QSPI_D1 - BOOTSEL	QSPI Data Line 1 and boot selection. To activate QSPI Master boot mode connect directly to QSPI Data Line 1 on Quad capable flash device	1	I/O
QSPI_D2	QSPI Data Line 2	60	I/O
QSPI_D3	QSPI Data Line 3	2	I/O
QSPI_CLK / SPI_CLK	QSPI Clock and SPI Clock	5	I/O

6.4.2 SPI slave boot mode

The boot mode is specified using QSPI_D1/BOOTSEL. If this pin is tied high via a 4.7k ohm resistor on start-up, the XVF3620 will enable SPI Slave boot mode and activate the pins shown below.

Table 13: SPI slave boot pins

Signal	Description	Comment	Pin	I/O
SPI_CLK	SPI Clock		5	I
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	6	I
SPI_MOSI	SPI Master Out Slave In		7	I
SPI_MISO	SPI Master In Slave Out	May be left floating if not required	47	O

6.5 Device firmware

Device Firmware Upgrade (DFU) is supported for devices that have QSPI flash connected and loaded with a firmware image. If the DFU process fails, the boot process safely falls back to the factory image allowing the user to re-attempt the upgrade. Images loaded via DFU can also be removed allowing the device to revert to the factory image.

7 Device characteristics

7.1 Electrical and Thermal characteristics

For electrical and thermal characteristics, including Absolute Maximum ratings please the *XU316-1024-QF60A* datasheet which contains electrical, design and integration data for the base processor.

8 Switching characteristics

For clock, reset and JTAG timing refer to the *XU316-1024-QF60A* datasheet. XVF3620 specific interface timings are detailed below.

8.1 QSPI Master (External flash for boot image storage)

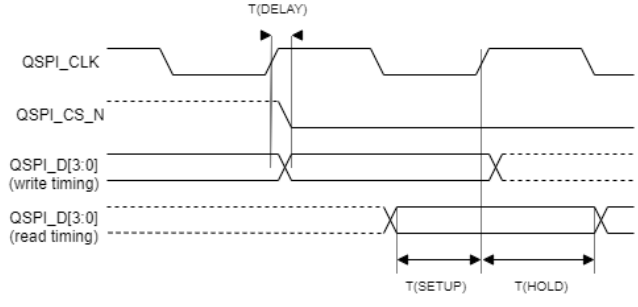

Fig. 10: QSPI Timing

Table 14: QSPI Timing Requirements

Parameter	Symbol	Min	Typi-cal	Max	Units
QSPI Clock frequency	f(QSPI_CLK)	-	15.6	-	MHz
QSPI_CLK to QSPI Data output delay	T(DELAY)	-2.7	-	2.7	ns
QSPI Data input to QSPI_CLK Setup time	T(SETUP)	22	-	-	ns
QSPI Data input to QSPI_CLK hold time	T(HOLD)	-11	-	-	ns

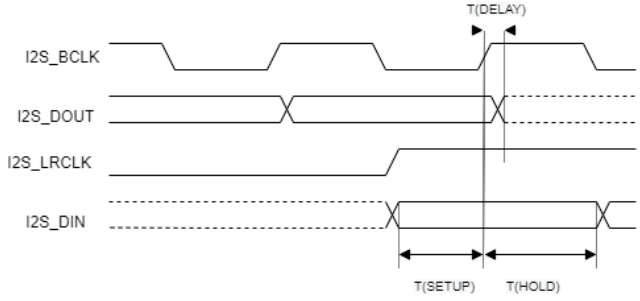

Fig. 11: I²S Slave timing

8.2 I2S Slave

Table 15: I²S Slave Timing Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Master clock input frequency	f(MCLKin)	-	12.288	24.576	MHz	A
I2S Bit Clock frequency input	f(I2S_BCLK)	1.024	-	3.072	MHz	
I2S Data Input (LRCLK) to I2S_BCLK setup time	T(SETUP)	0	-	-	ns	B
I2S Data Input (LRCLK) to I2S_BCLK hold time	T(HOLD)	6	-	-	ns	B
I2S_BCLK to I²S Data output delay	T(DELAY)	11	-	21.3	ns	

A: Configurable input multiplier used to generate appropriate audio sample rates (16kHz / 48kHz)

B: Timing also applies to I²S Sample Clock (I2S_LRCLK)

8.3 SPI Slave (External processor boot)

Table 16: SPI Slave Timing Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SPI Clock frequency	f(SPI_CLK)	-	12.5	-	MHz	
SPI_CLK to MISO output delay	T(DELAY)	11	-	21.3	ns	
SPI Master Output Slave Input (MOSI) to SPI_CLK Setup time	T(SETUP)	0	-	-	ns	
SPI Master Output Slave Input to (MOSI) SPI_CLK hold time	T(HOLD)	6	-	-	ns	

A: Timing also applies to SPI Chip Select input (SPI_CS_N)

9 Package information

9.1 Device markings

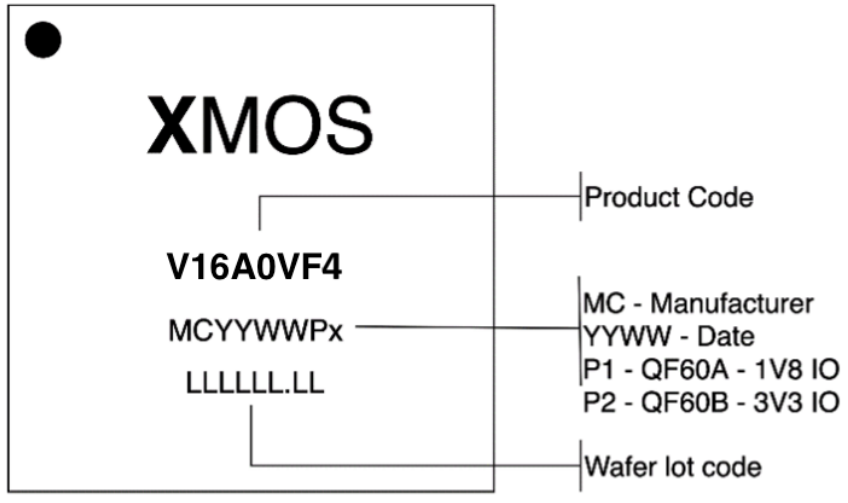

Fig. 12: Package marking for `XVF3620-QF60A-C`

9.2 Order codes

Table 17: Ordering code(s)

Product code	Marking **	Description
XVF3620-QF60A-C	V16A0VF4 MCYY- WWP1	Commercial Temp range (0 – 70 degrees Celsius) - 1.8V IO

9.3 Moisture Sensitivity Level

The package moisture sensitivity level rating is MSL-3. Devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Non-hermetic Solid-State Surface-Mount Devices (J-STD-020 Revision D).

9.4 Hazardous Materials

This product complies with the Reduction of Hazardous Substances (RoHS) directive. For details refer to the XMOS website: https://www.xmos.com/environmental.

10 Revision History

Table 18: Revision History

Version	Date	Comment
0.1.0	2025-10-15	First Preliminary Release
0.9.0	2026-01-29	Second Preliminary Release
1.0.0	2026-03-30	First public release
1.1.0	2026-06-09	Removed MC/EQ block from audio pipeline
1.1.1	2026-06-30	Corrected marking in Table 17: Ordering codes