USB Audio 2.0 Reference Design, XS1-L1 Edition Hardware Manual

REV 1.1

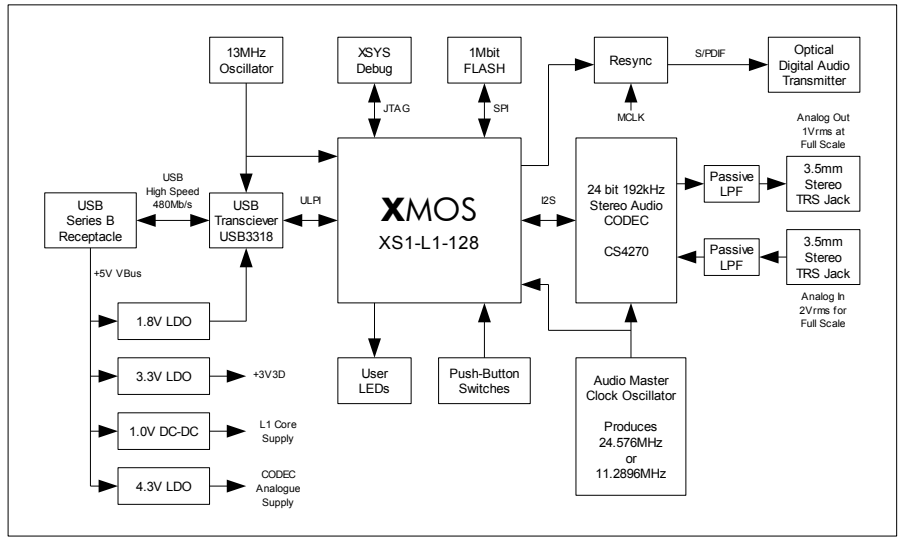
2010/04/26

XMOS

1 Introduction

The USB Audio 2.0 Reference Design, XS1-L1 Edition (hereafter "the board") is a hardware reference design for a USB audio interface using the XMOS XS1-L1 event-driven processor. It contains a single XS1-L1 device enabling implementation of a complete USB 2.0 high-speed device compliant with release 2.0 of the audio USB device class.

A block diagram of the design is shown below:



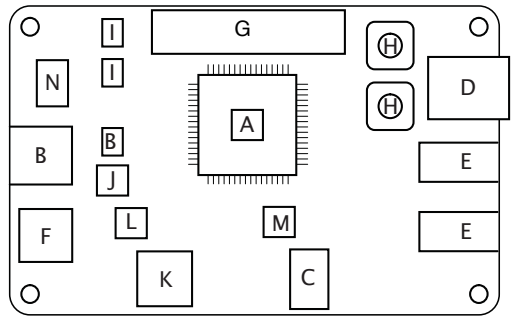
The XS1-L1 event-driven processor communicates with the USB host via a ULPI USB transceiver at the 480Mb/s high-speed rate. The XS1-L1 controls the streaming of audio data over the USB connection and direct I^2S interface to the audio CODEC. Multiple additional functions (e.g. Mixers/DSP etc.) can be implemented by modifications to the standard software.

Some key features of the board are listed below:

- USB bus-powered. No external power supply required
- Streams bit perfect audio data up to 24-bit @ 192kHz
- Supports standard sample rates - 44.1kHz, 48kHz, 88.2kHz, 96kHz, 192kHz
- USB endpoints use the asynchronous synchronisation mode to allow an external low jitter audio master clock to be used
- Optical digital audio output (S/PDIF)
- Stereo line level audio input and output

- XMOS XSYS debug header for easy programming/debug from the host using the XMOS XTAG2 debug adapter
- Two push-button switches and two LEDs for programmable use

The diagram below shows the layout of the main components on the board:



A	XS1-L1 Device	**H**	Push-Button Switch
B	USB Connector/Transceiver	**I**	Green User LED
C	Audio CODEC	**J**	USB Power LED
D	Optical digital output	**K**	Audio Clocking
E	3.5mm Stereo Jack	**L**	1V0 Core Supply
F	SPI FLASH	**M**	4V3 Analogue Supply
G	XSYS Debug Interface	**N**	13MHz Oscillator

The rest of this document provides a detailed description of each of the main circuit components.

2 XS1-L1 Device [A]

The board is based on a single XS1-L1 device in a 128 pin TQFP package.

The XS1-L1 consists of a single XCore, which comprises an event-driven multi-threaded processor with tightly integrated general purpose I/O pins and 64 KBytes of on-chip RAM and 8 KBytes of OTP (One Time Programmable) memory.

The processor has time-aware ports that are directly connected to the I/O pins. Examples of how to write software that interfaces over these ports is provided in *Programming XC on XMOS Devices*.

2.1 Clocking

A discrete 13MHz oscillator is used to feed the XS1-L1 reference clock input and also the USB3318 USB transceiver. The L1 has the MODE1 and MODE0 pins wired to ground which sets the internal XS1-L1 PLL multiplication factor to 30.75. This results in a core clock frequency of 399.75MHz and an I/O reference clock frequency of 99.9375MHz.

2.2 Reset

A supply voltage supervisor connected to the 1V0 core supply is used to provide a power on reset signal. This signal is buffered and wired to the RST_N and TRST_N pins of the L1. This ensures the device will be reset at power on and also provides predictable behaviour under brownout conditions. The device can also be reset over the XSYS debug interface.

2.3 Boot

The boot mode of the device is set by the MODE3 and MODE2 pins which are connected together on the board. With MODE3 and MODE2 both high (default), the device will boot from the 1Mb SPI FLASH on the board. With MODE3 and MODE2 both low, the device will not boot from SPI FLASH allowing boot instead via JTAG over the XSYS debug link.

Without anything connected to the XSYS interface, the board will boot from SPI FLASH. With the XTAG2 connected to the XSYS interface, the host can control the boot mode of the device by way of the TRST_N line.

3 USB Connector and Transceiver [B]

The board uses a standard USB series B receptacle as its USB connector. The high-speed USB signals are connected to an SMSC® USB3318 USB transceiver which provides a ULPI connection to the XS1-L1.

On power-up, a pulldown resistor holds the transceiver in reset until the XS1-L1 is ready to begin accepting USB traffic. The USB transceiver reset pin is connected to bit zero of port 32A so this can be controlled by software.

The transceiver uses the 13MHz clock provided by a discrete oscillator on the board which doubles as the reference clock for the XS1-L1.

The I/O pins for the USB transceiver are mapped to ports on the XS1-L processor as described in the port map shown later in this document.

4 Audio CODEC [C]

The board uses a 24 bit, 192kHz stereo audio CODEC (Cirrus Logic® CS4270).

The CODEC is configured to operate in stand-alone mode meaning that no serial configuration interface is required. The digital audio interface is set to I^2S mode with all clocks being inputs (slave mode).

The CODEC has three internal modes depending on the sampling rate used. These change the oversampling ratio used internally in the CODEC. The three modes are shown below:

CODEC mode	CODEC sample rate range
Single speed	4-54kHz
Double speed	50-108kHz
Quad speed	100-216kHz

In stand-alone mode, the CODEC automatically determines which mode to operate in based on the input clock rates.

The internal master clock dividers are set using the MDIV pins. MDIV1 is tied low and MDIV2 is controlled by the L1 on bit 2 of port 32A.

With MDIV2 low, the master clock must be 256Fs in single speed mode, 128Fs in double speed mode and 64Fs in quad speed mode. This allows an 11.2896MHz master clock to be used for sample rates of 44.1, 88.2 and 176.4kHz.

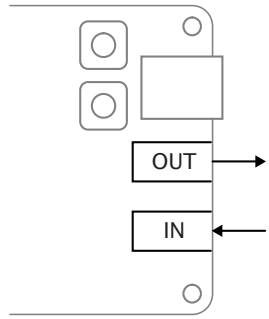
With MDIV2 high, the master clock must be 512Fs in single speed mode, 256Fs in double speed mode and 128Fs in quad speed mode. This allows a 24.576MHz master clock to be used for sample rates of 48, 96 and 192kHz.

These master clock frequencies were chosen due to the easy availability of crystals at these frequencies.

The reset pin on the CODEC is mapped to bit 1 of port 32A on the processor.

4.1 Audio IO

Two 3.5mm Tip Ring Sleeve (TRS) audio jacks are provided for stereo audio input and output. The layout of the audio jacks is displayed below:



A simple passive ac-coupling and low pass filter circuit is used on input and output. The circuit is configured so that the audio output will produce approximately $1V_{RMS}$ (0dBV) for a digital full scale signal. Due to the output coupling capacitors, the output impedance falls with frequency and is approximately 1kΩ @ 35Hz falling to 576Ω @ 1kHz.

The input circuit contains an attenuator such that a $2V_{RMS}$ (+6dBV) signal will produce a full scale digital output. The input impedance is approximately 8kΩ.

5 Optical digital output [D]

An optical digital audio transmitter is used to provide a digital audio output in IEC60958 consumer mode (S/PDIF) format. The S/PDIF signal is generated from a 1-bit port on the processor as defined in the port map. The data stream from the L1 is reclocked using the external master clock to synchronise the data into the audio clock domain. This is achieved using a simple external D-type flip-flop.

6 SPI Flash Memory [F]

The board contains a 1Mbit FLASH memory device which is connected via a standard Serial Peripheral Interface (SPI).

The FLASH is connected to four 1-bit ports as shown in the port map. These are the standard ports the processor will try to boot from in boot from SPI mode.

Three of these ports are shared with I^2S digital audio signals therefore the FLASH cannot be accessed at the same time as digital audio is playing. When accessing the SPI FLASH, the CODEC is held in reset and it ignores the three inputs shared with SPI signals. When digital audio is playing, the FLASH is deselected by holding its chip select (slave select) line inactive. In this mode, the FLASH will ignore other input signals and set its output high impedance therefore it does not affect the shared signals. The slave select signal is only active when booting the device therefore and is held inactive while audio is playing.

The XMOS development tools include the XFLASH utility for programming compiled programs into the flash memory. Software may also access the FLASH memory at run-time by interfacing with the above ports. Note that, as mentioned, this can not happen simultaneously with audio IO.

7 XSYS Interface [G]

A standard XMOS XSYS interface is provided to allow host debug of the board via JTAG.

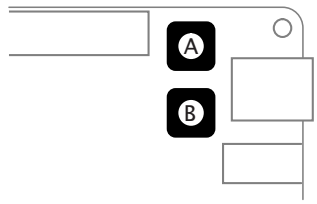
An XTAG2 USB debug adapter can be plugged into this port to allow running/debugging code, programming the FLASH memory and selection of boot mode. A 20-way IDC header is used as the physical connector and the pinout of this is shown below:

Signal	Pin	Description
TRST_N	3	JTAG Test Reset. Active low.
TMS	7	JTAG Test Mode Select.
TCK	9	JTAG Test Clock.
TD1	5	JTAG Test Data. From debug adapter to XS1-L1.
TD2	13	JTAG Test Data. From XS1-L1 to debug adapter.
SRST_N	15	System Reset. Active low. Resets XS1-L1 device.
DEBUG	11	XS1-L1 DEBUG Interrupt line.
GND	4, 8, 12, 16, 20	Ground.
NC	1, 2, 6, 10, 14, 17, 18, 19	These pins are not connected.

On power on, the XS1-L1 boots from the on-board flash memory. With the XTAG2 connected, the XS1-L1 can be reset and then booted from a program on the host PC.

8 Push-Button Switches [H]

The board provides two push-button switches whose states can be sampled at any time by software. The layout of these switches is shown below:

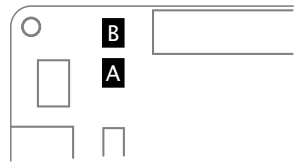


The switches are connected to two 1-bit ports, the mapping of which can be seen in the port map.

The port will go logic low when the button is pressed.

9 User LEDs [I]

The board provides two user LEDs that can be driven by software. The layout of these LEDs is shown below:



The LEDs are connected to two bits of port 32A as shown in the port map. Setting the relevant bit high will turn the LED on.

10 Power

The board is a high-power bus-powered USB device. This means all the power used by the board is derived from the nominally +5V VBus supply from the USB connector and that the device will use more than 100mA from the VBus line when configured. The board will use approximately 150mA when fully configured and operating.

Simple Low drop out (LDO) linear regulators are used to generate the global 3.3V supply and the 1.8V supply required by the USB3318 USB transceiver.

A low noise LDO regulator is used to generate the analogue supply for the Audio CODEC. The CODEC offers higher audio performance at higher supply voltages so the voltage for this supply is set at 4.3V. This allows some headroom between the 4.5V minimum VBus voltage and the approx 100mV dropout of the LDO + RC pre-filter.

A low cost buck switching regulator is used to generate the 1.0V core supply for the XS1-L1. A ferrite bead is used on the +5V VBus input to prevent switching noise propagating down the USB cable.

The 3V3 and 1V0 supplies are sequenced by using the power good signal from the 3V3 regulator as the enable input of the 1V0 DC-DC regulator. This ensures 3V3 is in regulation before the 1V0 supply turns on as required by the device.

When the board is correctly connected to a USB source the USB Power LED is illuminated.

11 Audio Clocking [K]

The audio USB endpoints are configured in asynchronous mode. This means that the board acts as the audio clock master and the host as the slave. This has the benefit that a simple crystal oscillator can be used to generate the audio master clock which typically results in lower jitter and consequently higher quality audio.

Two crystal oscillators are used on the board to support the two standard sample rate base frequencies (44.1 and 48kHz). The crystal oscillators are built using discrete components for low cost and easy availability however standard canned oscillators could also be used. The oscillator design is a simple Pierce oscillator using an unbuffered inverter as the amplifying component. The MCLK_SEL signal selects which of the two oscillators is enabled, only one is enabled at any one time to avoid any interference from the unused clock.

The behaviour of this select signal is shown below:

MCLK_SEL	Audio master clock frequency
0	11.2896MHz
1	24.576MHz

The audio master clock is connected to a 1-bit port of the XS1-L1 so that all of the I^2S outputs are synchronised with it. This also allows the S/PDIF output to be generated from a buffered 1-bit port clocked by the audio master clock input.

The MCLK_SEL signal is mapped to bit 2 of port 32A on the processor as shown in the port map.

12 Test Points

The board provides 18 through-hole test points as defined in the table below:

Test Point	Port	Signal
1	P1I0	CODEC_ADC_DATA
2	P1D0	SPI_MOSI / CODEC_DAC_DATA
3	P1A0	SPI_MISO / CODEC_SCLK
4	P1C0	SPI_CLK / CODEC_LRCK
5	NA	CODEC_MCLK
6	P32A2	MCLK_SEL
7	P32A1	CODEC_RST_N
8	NA	GND
9	P1L0	SPDIF_TX
10	NA	SPDIF_OUT
11	P32A6	XD55
12	P32A7	XD56
13	P32A8	XD57
14	P32A9	XD58
15	P32A10	XD61
16	NA	3V3
17	NA	5V
18	NA	4V3A

13 Printed Circuit Board

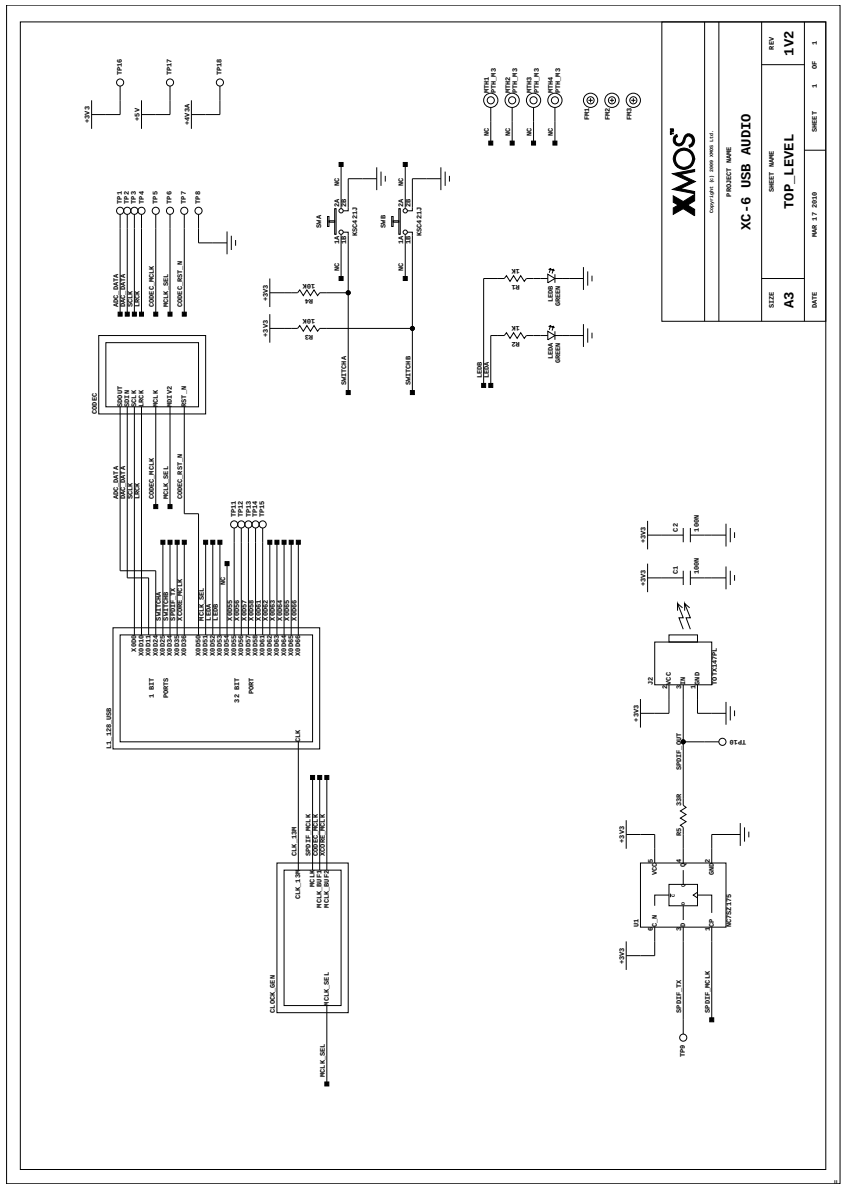
The PCB is a two layer design in a credit card form factor with dimensions of 86 x 54mm. The mounting holes are 3.2mm in diameter.

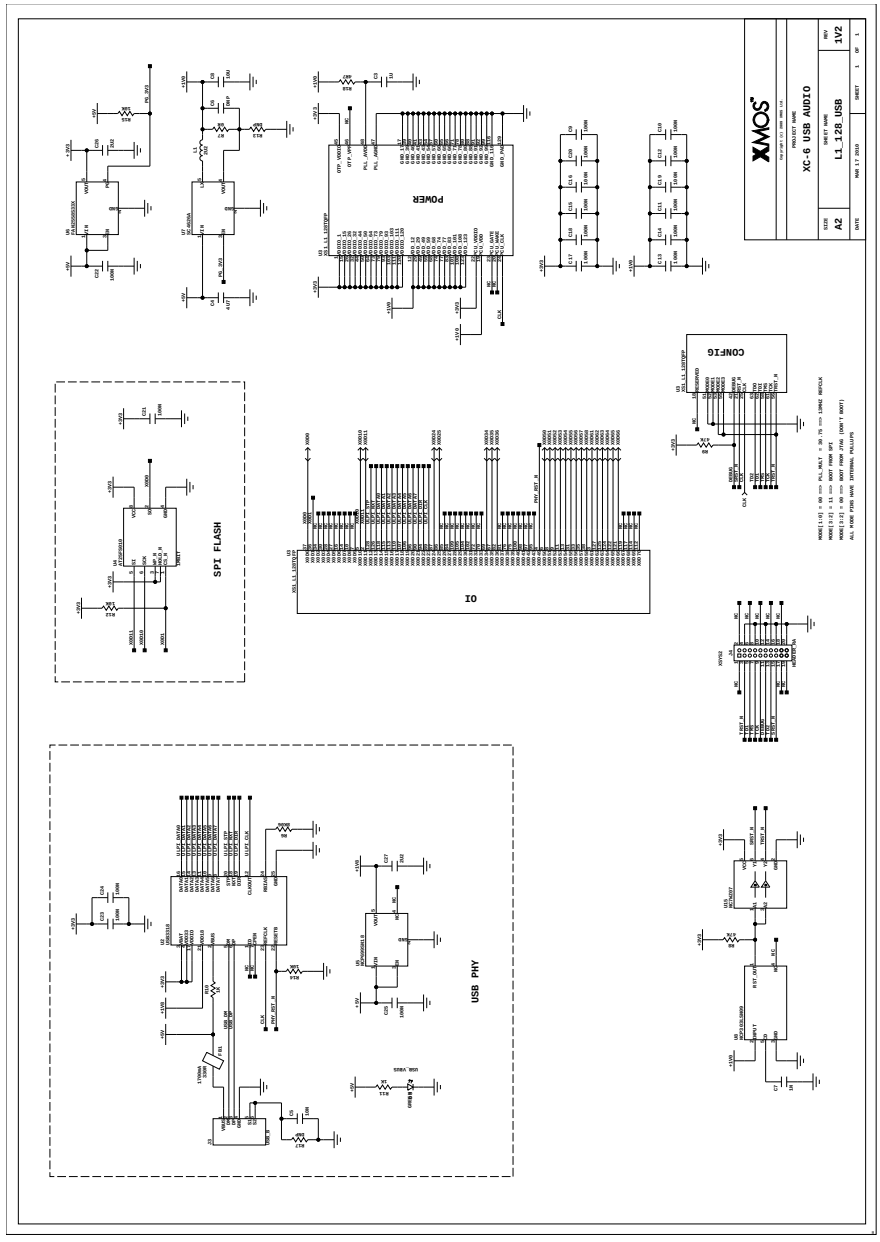
14 Port Map

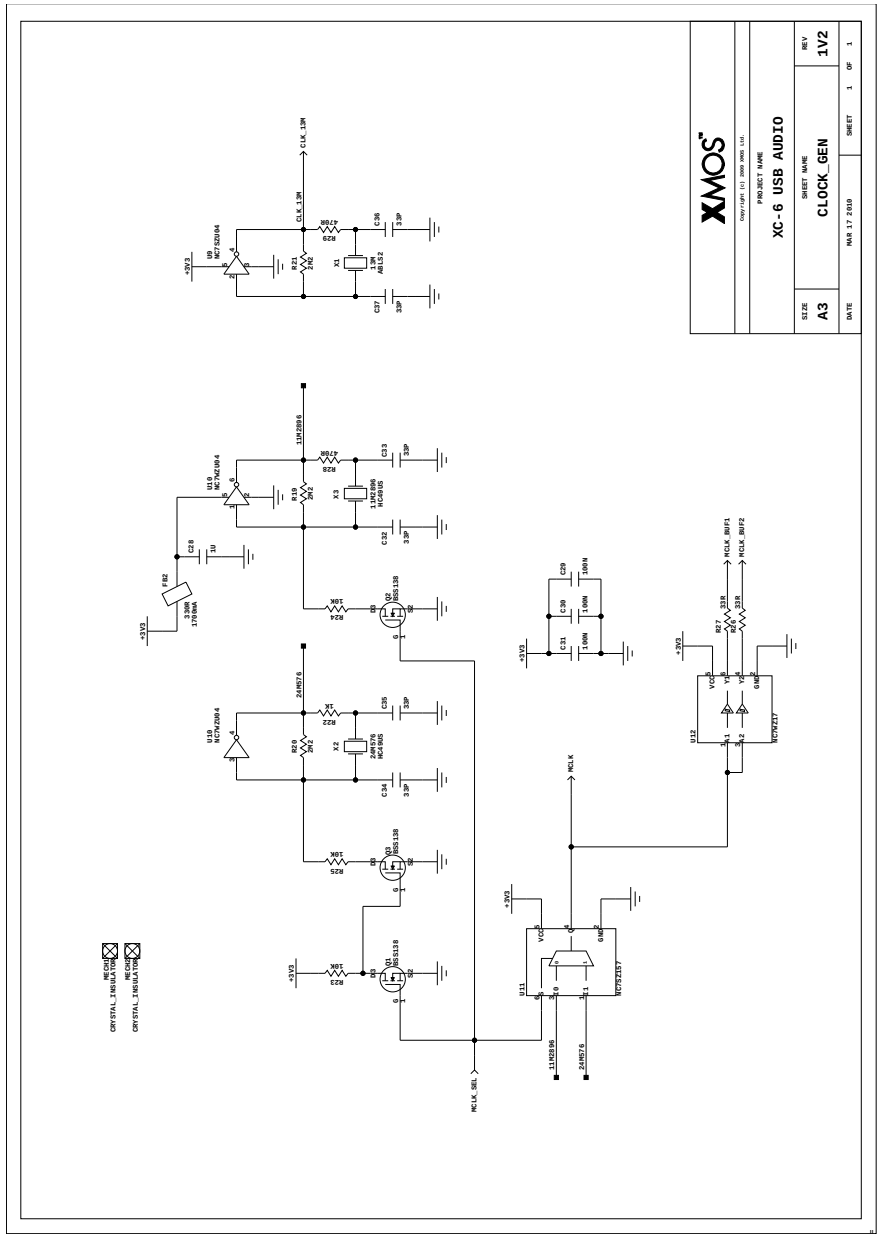
The table on the following page provides a full description of the port to signal mappings used on the board.

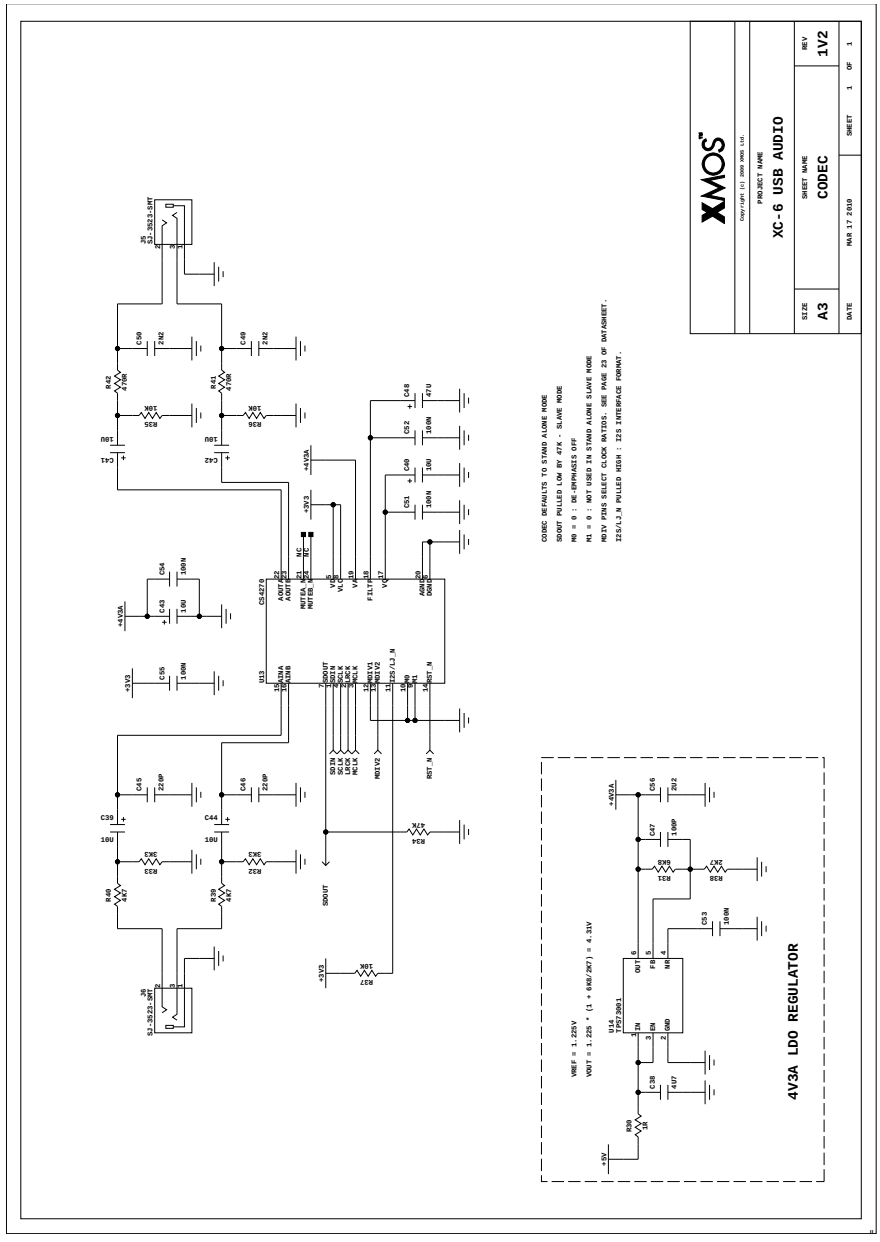
Package	Ports					Signals
Pin Name	1b	4b	8b	16b	32b	
XnD0	P1A0					SPI_MISO / CODEC_SCLK
XnD1	P1B0					SPI_SS
XnD2		P4A0	P8A0	P16A0	P32A20	Not available in ULPI mode
XnD3		P4A1	P8A1	P16A1	P32A21	
XnD4		P4B0	P8A2	P16A2	P32A22	
XnD5		P4B1	P8A3	P16A3	P32A23	
XnD6		P4B2	P8A4	P16A4	P32A24	
XnD7		P4B3	P8A5	P16A5	P32A25	
XnD8		P4A2	P8A6	P16A6	P32A26	
XnD9		P4A3	P8A7	P16A7	P32A27	
XnD10	P1C0					SPI_CLK / CODEC_LRCK
XnD11	P1D0					SPI_MOSI / CODEC_DAC_DATA
XnD12	P1E0					ULPI_STP
XnD13	P1F0					ULPI_NXT
XnD14		P4C0	P8B0	P16A8	P32A28	ULPI_DATA0
XnD15		P4C1	P8B1	P16A9	P32A29	ULPI_DATA1
XnD16		P4D0	P8B2	P16A10		ULPI_DATA2
XnD17		P4D1	P8B3	P16A11		ULPI_DATA3
XnD18		P4D2	P8B4	P16A12		ULPI_DATA4
XnD19		P4D3	P8B5	P16A13		ULPI_DATA5
XnD20		P4C2	P8B6	P16A14	P32A30	ULPI_DATA6
XnD21		P4C3	P8B7	P16A15	P32A31	ULPI_DATA7
XnD22	P1G0					ULPI_DIR
XnD23	P1H0					ULPI_CLK
XnD24	P1I0					CODEC_ADC_DATA
XnD25	P1J0					SWITCH_A
XnD26		P4E0	P8C0	P16B0		Not available in ULPI mode
XnD27		P4E1	P8C1	P16B1		
X0D28		P4F0	P8C2	P16B2		
X0D29		P4F1	P8C3	P16B3		
X0D30		P4F2	P8C4	P16B4		
X0D31		P4F3	P8C5	P16B5		
XnD32		P4E2	P8C6	P16B6		
XnD33		P4E3	P8C7	P16B7		
XnD34	P1K0					SWITCH_B
XnD35	P1L0					SPDIF_TX
XnD36	P1M0		P8D0	P16B8		MCLK_IN
XnD37	P1N0		P8D1	P16B9		Not Available in ULPI mode
XnD38	P1O0		P8D2	P16B10		
XnD39	P1P0		P8D3	P16B11		
XnD40			P8D4	P16B12		
XnD41			P8D5	P16B13		
XnD42			P8D6	P16B14		
XnD43			P8D7	P16B15		
XnD49					P32A0	USB_PHY_RST_N
XnD50					P32A1	CODEC_RST_N
XnD51					P32A2	MCLK_SEL
XnD52					P32A3	LED_A
XnD53					P32A4	LED_B
XnD54					P32A5	NC
XnD55					P32A6	TESTPOINT
XnD56					P32A7	TESTPOINT
XnD57					P32A8	TESTPOINT
XnD58					P32A9	TESTPOINT
XnD61					P32A10	TESTPOINT
XnD62-70					P32A[19:11]	NC

15 Schematics




XC-6 USB AUDIO
SHEET NAME
L1_128_USB
REV
1V2
SIZE
A2
DATE
Mar 17 2010
SHEET
1
OF
1
POWER
IO
CONFIG
SPI FLASH
USB PHY
MODE[1:0] = 00 ==> PLL_REF = 20 MHz ==> 13MHz REFCLK
MODE[2:1] = 11 ==> BOOT FROM SPI
MODE[2:0] = 00 ==> BOOT FROM JTAG (DON'T BOOT)
ALL MODE PINS HAVE INTERNAL PULLUPS


XMOS
XC-6 USB AUDIO
CLOCK_GEN
1V2
A3
MAR 17 2010
CLK_13M
MCLK
MCLK_SEL
MCLK_RFF1
MCLK_RFF2
+3V3
11M2896
24M576
CRYSTAL_INSULATOR
MECHANICAL


XMOS
XC-6 USB AUDIO
CODEC
1V2
A3
MAR 17 2010
CODEC DEFAULTS TO STAND ALONE MODE
SDOUT PULLED LOW BY 47K - SLAVE MODE
M0 = 0 : NO-EMPHASIS OFF
M1 = 0 : NOT USED IN STAND ALONE SLAVE MODE
M3V PINS SELECT CLOCK RATIOS. SEE PAGE 23 OF DATASHEET.
I2S/LJ_N PULLED HIGH : I2S INTERFACE FORMAT.
4V3A LDO REGULATOR
VREF = 1.225V
VOUT = 1.225 * (1 + 66K/2K7) = 4.31V
U13
CS4270
U14
TPS73001
SDOUT

16 Document History

Date	Release	Comment
2009-10-05	1.0	Original version.
2010-04-26	1.1	Updated for 1V2 version of board. Power supply sequencing description added. Power on reset circuit description updated. Full port map updated.

17 Related Documents

The following documents provide more information on designing with the USB Audio 2.0 Reference Design, XS1-L1 Edition:

- *Programming XC on XMOS Devices*: explains how to program XMOS event-driven processor devices using the XC language.
- *XCore XS1 Architecture Tutorial*: provides an overview of the XS1 instruction set architecture.
- *XS1 XSystem-L*: provides an introduction on how to boot the XS1-L devices.
- *XMOS Tools User Guide*: explains how to use the XMOS Tools to program XMOS event-driven processor devices.

The most up-to-date information on the board, including schematics and product datasheets, is available from:

- `http://www.xmos.com/usbaudio2/`