XMOS XVF3800 - Datasheet

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XMOS

Table of Contents

1 Key Features

The VocalFusion® XVF3800 is a high-performance voice processor that is optimised for voice communications with the following key features.

1.1 Voice Processing

- Four PDM microphone interfaces
- Digital signal processing pipeline
- Full duplex Acoustic Echo Cancellation (AEC)
- Fast tracking or fixed Beamformer with multiple beams
- Dynamic Echo and Noise suppressor
- Automatic Gain Control (AGC)
- Limiter
- Indication of Direction of Arrival (DoA)
- Automatic Speech Recognition (ASR) output with a configurable fixed gain

1.2 Device Interfaces

- High speed USB2.0 compliant device supporting USB Audio Class (UAC) 2.0
- Reference audio via I^2S or USB
- USB Endpoint 0 vendor specific device class based control interface
- I^2C or SPI control interfaces

1.3 Firmware Management

- Boot from QSPI Flash
- Default firmware image for power-on operation
- Update image delivered via USB DFU or I^2C
- Option to boot from a local host processor via SPI

1.4 Package

- 7 mm x 7 mm 60 pin QFN package

1.5 Power Consumption

- Typical core (VDD) power consumption: 345 mW (I2S) / 400 mW (USB)

2 Product Overview

2.1 Introduction

The XMOS VocalFusion ® XVF3800 is a high-performance voice processor that uses microphone array processing and a sophisticated audio processing pipeline to capture clear, high-quality speech from anywhere in a room. The XVF3800 uses the XMOS xcore.ai processor and supports a range of integrated and accessory voice communication applications.

The XVF3800 is a highly customisable design that combines an XMOS processor and application firmware into a single solution. It offers system designers the flexibility to integrate the XVF3800 into different designs. The xcore.ai processor has a powerful architecture which delivers high performance, real-time audio processing while the XVF3800 firmware is designed to be easily customized, allowing users to modify it as required.

In addition to the audio processing functions, the XVF3800 includes a range of standard interfaces that enable it to be connected to a wide variety of devices. It supports a simple, intuitive control interface that enables designers to quickly and easily configure the system and perform common tasks.

The overall system context for the XVF3800 is shown below. In most applications the XVF3800 device will operate in conjunction with an external host processor.

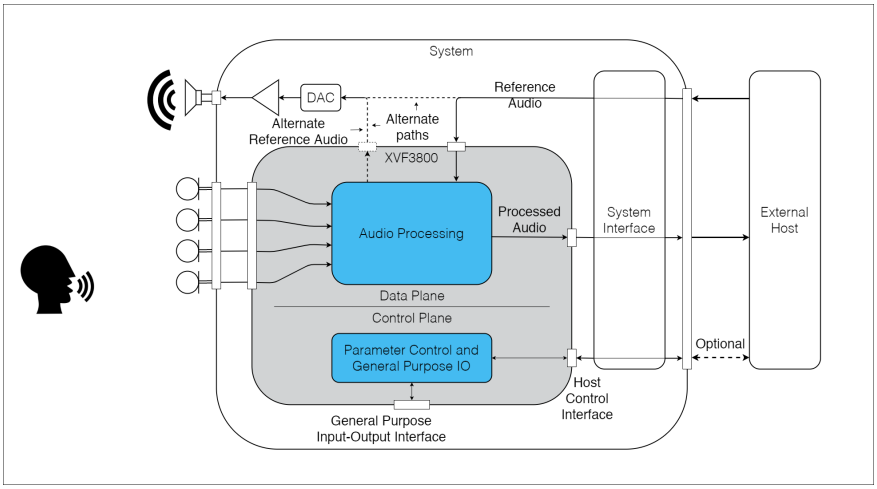


Fig. 2.1: XVF3800 device system context

This datasheet describes the main functional blocks in the XVF3800 and includes a reference configuration for the device. Details of the firmware features and the configuration and customisation options are provided in the XVF3800 User Guide.

Important:

The information in this datasheet should be read in conjunction with the XU316-1024-QF60B datasheet which contains electrical, design and integration data for the xcore.ai processor.

2.2 Voice Processing

The XVF3800 voice processor converts and enhances audio captured using four low-cost digital microphones. Processed audio streams are suitable for use in voice communications applications and benefit from a range of configurable audio processing techniques to allow customisation to the use case. The embedded audio processing provides the following features:

- 4 microphone far-field operation.
- Full 360-degree and 180-degree operation depending on microphone geometry.
- 16 kHz voice processing, with optional 16 kHz and 48 kHz interface sampling rates.
- Full duplex, mono, Acoustic Echo Cancellation accommodating highly reverberant environments. (Reference audio for cancellation provided via either an I^2S or USB interface).
- Configurable bulk delay insertion to account for audio delays ensuring optimal echo cancellation with all audio output paths.
- Multi-beamforming and de-reverberation with coherent addition and suppression of room reflections through energy harvesting.
- Removal of coherent point noise sources using generalized side-lobe cancellation.
- Stationary and non-stationary dynamic echo and noise suppression.
- Adjustable gain over a 60 dB range with automatic gain control.
- Audio output filtering and range limiter.
- Indication of Direction of Arrival (DoA) for the selected speaker.

2.3 Peripheral Interfaces

The XVF3800 voice processor provides the following additional interfaces to increase usability and reduce total system cost:

- 5 General Purpose Output (GPO) pins. These can be configured as simple digital I/O pins, Pulse Width Modulated (PWM) outputs and rate adjustable LED flashers.
- 2 General Purpose Input (GPI) pins. These can be used as simple logic inputs or event capture (edge detection).

These GPO can be controlled and the GPI states read by the host system over the control interface (SPI, I^2C or USB, depending on the firmware configuration). A range of triggering conditions are supported and the INT_N output can be used to signal an interrupt to the host system when a GPI is triggered. The XVF3800 allows for the extension of the number of GPIO pins listed above, by using the I^2C-to-IO expander feature. See the XVF3800 User Guide for further information.

2.4 System Firmware

The VocalFusion XVF3800 voice processor can be booted over SPI by a local host processor or from a separate, user-supplied, QSPI Flash memory.

Note: The two XVF3800 configurations: one providing I^2S/I^2C/SPI interface (XVF3800-INT) and one providing a USB interface (XVF3800-UA) are delivered as separate sets of firmware.

2.5 System Configurations

The XVF3800 can be configured to operate in a number of system designs and supports a range of interfaces. The main configurations are:

Table 2.1: XVF3800 system configurations

Config	Application	Audio	Control
INT-Device UA	Integrated voice processor USB Accessory	I^2S USB UAC 2.0	SPI or I^2C USB Endpoint 0

The control interface is optional - the XVF3800 can be configured with optimised audio parameters as the default power-on settings.

Functional block diagrams of the XVF3800 in typical integrated and USB accessory applications are shown in the figures below.

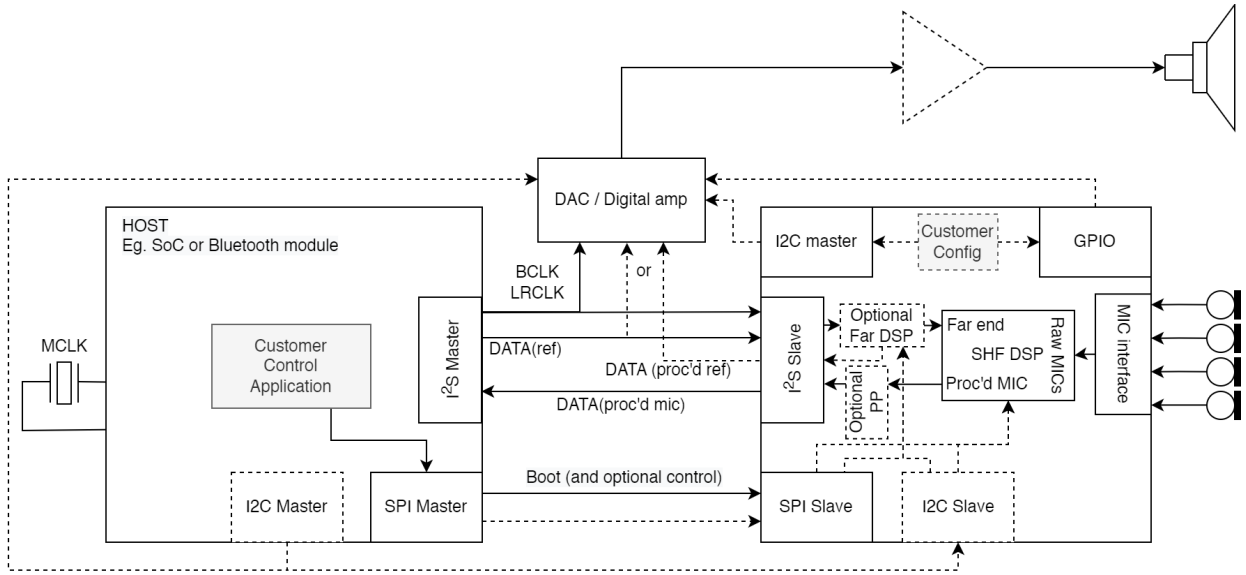


Fig. 2.2: Functional block diagram of XVF3800 in INT-Device configuration

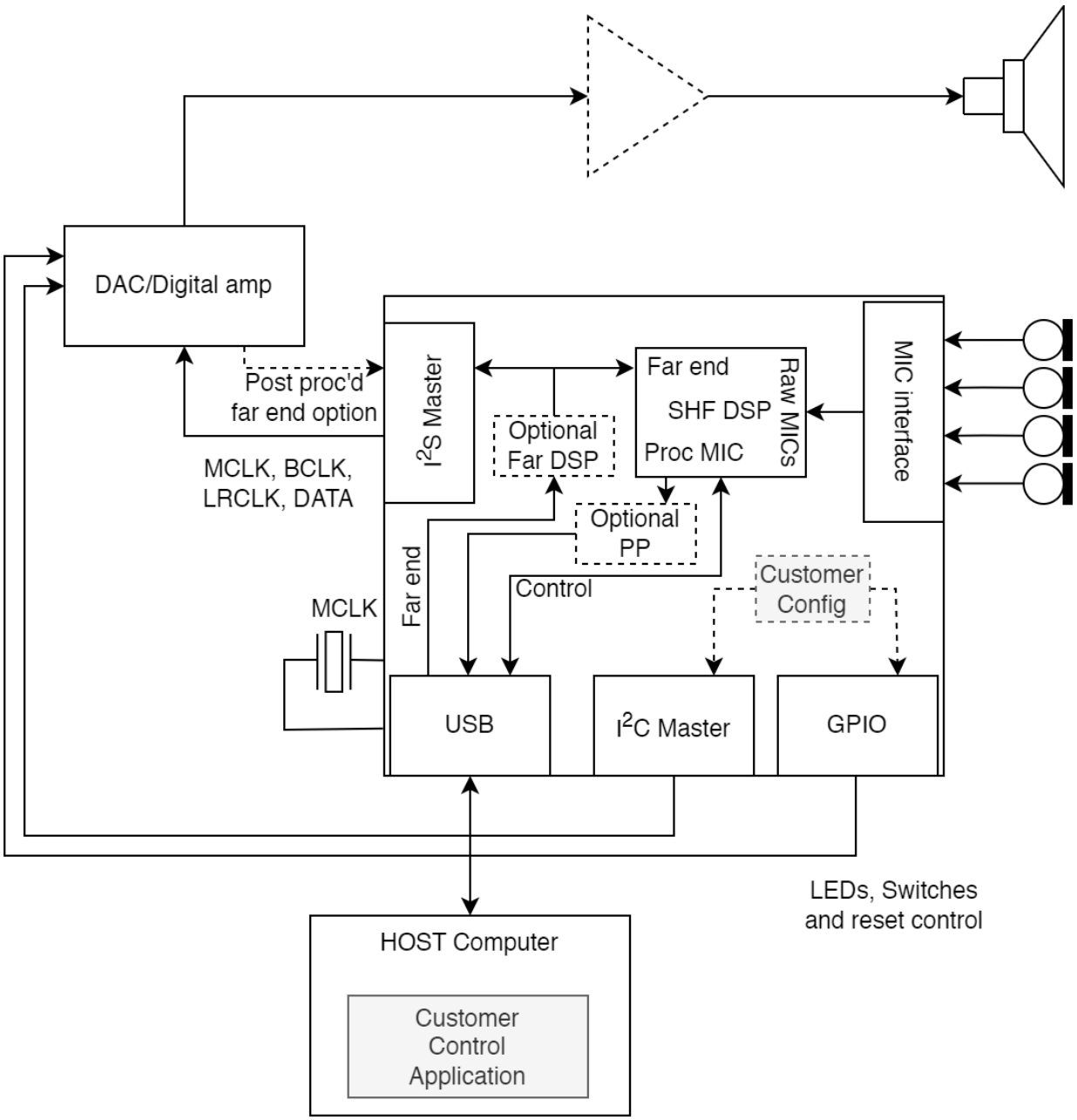


Fig. 2.3: Functional block diagram of XVF3800 in UA configuration

3 Voice Processing Pipeline

3.1 Overview and Key Features

The XVF3800 integrates a set of advanced Digital Signal Processing (DSP) algorithms that include Acoustic Echo Cancellation (AEC), beamforming, dereverberation, noise suppression and automatic gain control. These advanced DSP algorithms deliver high speech-to-noise ratio, naturally sounding speech and eliminate acoustic echo while maintaining a transparent and low latency communication link.

The key features of the XVF3800 solution are:

- High levels of Acoustic Echo Cancellation and Suppression in conferencing and living room conditions.
- State of the art, robust, and natural double-talk / full-duplex performance.
- High speech clarity level even when users are at several meters distance, without requiring directional microphones.
- Fast adaptive beamforming for tracking multiple near-end users.
- Stationary / diffuse noise suppression.
- Automatic gain control.

3.2 Main Functional Blocks

A high level diagram of the solution is shown below.

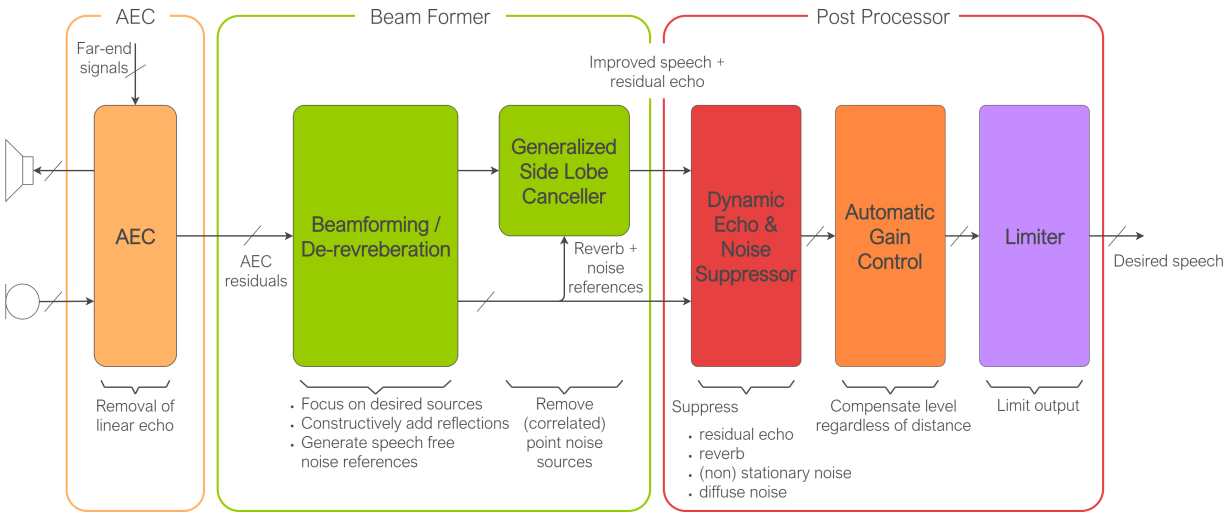


Fig. 3.1: Voice processing pipeline

3.2.1 Microphone Inputs

The XVF3800 captures voice signals through four digital microphones and converts them from Pulse Density Modulation (PDM) to Pulse Code Modulation (PCM). It passes the converted signals to the voice pipeline, along with the far-end signal that is played on the loudspeaker after having passed through a Digital to Analog Converter (DAC) and amplifier.

3.2.2 Acoustic Echo Canceller

The first stage of the processing pipeline is the Acoustic Echo Canceller (AEC) which uses an adaptive filter to remove the echos of the far end signal from the microphone signals. Each of the microphone signals is processed independently and the output of the AEC is feed into the beamformer.

At startup the AEC calibrates the adaptive filters to match the acoustic path between the loudspeaker and the microphones. This requires some far end audio content to provide a signal to the device. If the AEC detects a significant change to the acoustic path during operation, e.g. if the device is moved, it will initiate a re-convergence operation.

3.2.3 Beamformer

The beamformer block processes the AEC signals to select the desired speaker. The beamformer contains a set of adaptive filters that coherently add signals from the four microphones to select sounds from a specific direction. This operation enhances the speech to noise level in a specific direction and simultaneously reduces the effects of point noise sources and reverberation effects.

The XVF3800 implements three beams - one free running beam that scans the environment for new speakers, and two focused beams that can track individual speakers. An alternative operating mode is also supported in which both focused beams can be fixed to a user specified azimuth angle. The final stage of the pipeline automatically selects which beam to use as the output from the device.

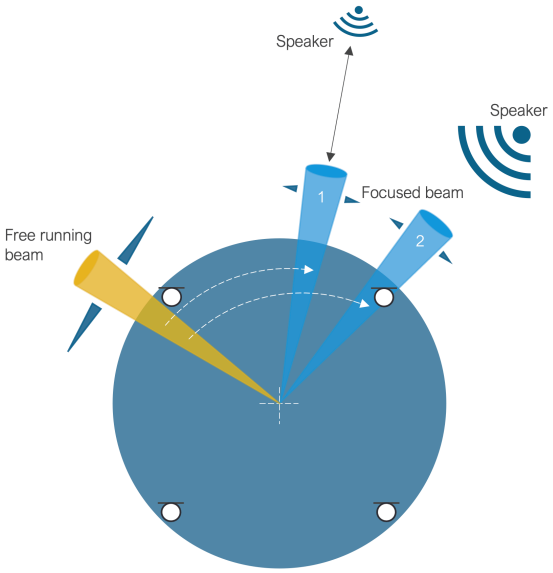


Fig. 3.2: Beamformer Operation

It is possible to access information on the selected beams from the XVF3800 control interface. The device provides a Direction of Arrival (DoA) measurement indicating the direction of the selected beam.

3.2.4 Post Processor

Outputs from the beamformer are fed to the post processing stage which further reduces reverberation and suppresses diffuse and point noise sources. This is followed by a programmable equalization filter to adjust the frequency response of the output signal, and gain control block which ensures a consistent output level regardless of the distance of the speaker from the microphone. The final output is passed through a limiter to ensure that any very loud signals do not overload the output.

The output from this pipeline is an enhanced speech signal of the desired near-end speech without echo and reverberation.

3.3 Automatic Speech Recognition (ASR) output

The output of the beamformer can be used as an input to an Automatic Speech Recognition (ASR) engine. In this mode the XVF3800 provides a configurable fixed gain to adapt the input level to the ASR engine.

3.4 Input and Output

The XVF3800 supports two types of audio interface to transport audio to and from the host system; I^2S or USB. These are mutually exclusive and selected when the firmware image is built.

3.4.1 I^2S Audio Interface

The XVF3800 supports I^2S sample rates of 16 kHz or 48 kHz. Both input and output must use the same rate.

The audio pipeline processes data with a sample rate of 16 kHz so, if 48 kHz inputs are used, a Sample Rate Converter block is introduced into the signal path to adapt the rates. The sample rates are set in the firmware and cannot be changed during operation of the device. The bit depth of the samples is fixed at 32 bits.

When used in UA mode (host audio over USB) the XVF3800 has an active I^2S master output which provides the far end signal to the DAC.

3.4.2 USB Audio Interface

The XVF3800 implements a standard UAC 2.0 audio class in Adaptive Mode which is compatible with USB hosts supporting USB 2.0 and 3.0 interfaces. All major operating systems now support USB Audio Class 2 (UAC 2) devices natively without the requirement to install additional audio drivers.

In the UA configuration the XVF3800 audio sample rate can be either 16 kHz or 48 kHz (fixed at build time) and must be the same as the output rate used for the DAC attached to the I^2S output. The bit depths of the USB samples can be either 16, 24, or 32 (fixed at build time).

3.4.3 Reference Signal for AEC

The XVF3800 supports a monophonic audio output and uses a single channel to provide the reference signal for the acoustic echo canceller (AEC). A far-end AEC reference signal must be provided on the left (0) channel of the I^2S or USB input signal. Data on the right channel is ignored. In order to ensure the far end that is playing into the room matches the far-end that the AEC is expecting, the DAC is configured to play the left input channel on both the right and left outputs.

3.5 Key parameters

The key operating parameters of the audio processing pipeline are shown in the table below.

Table 3.1: Pipeline paramenters

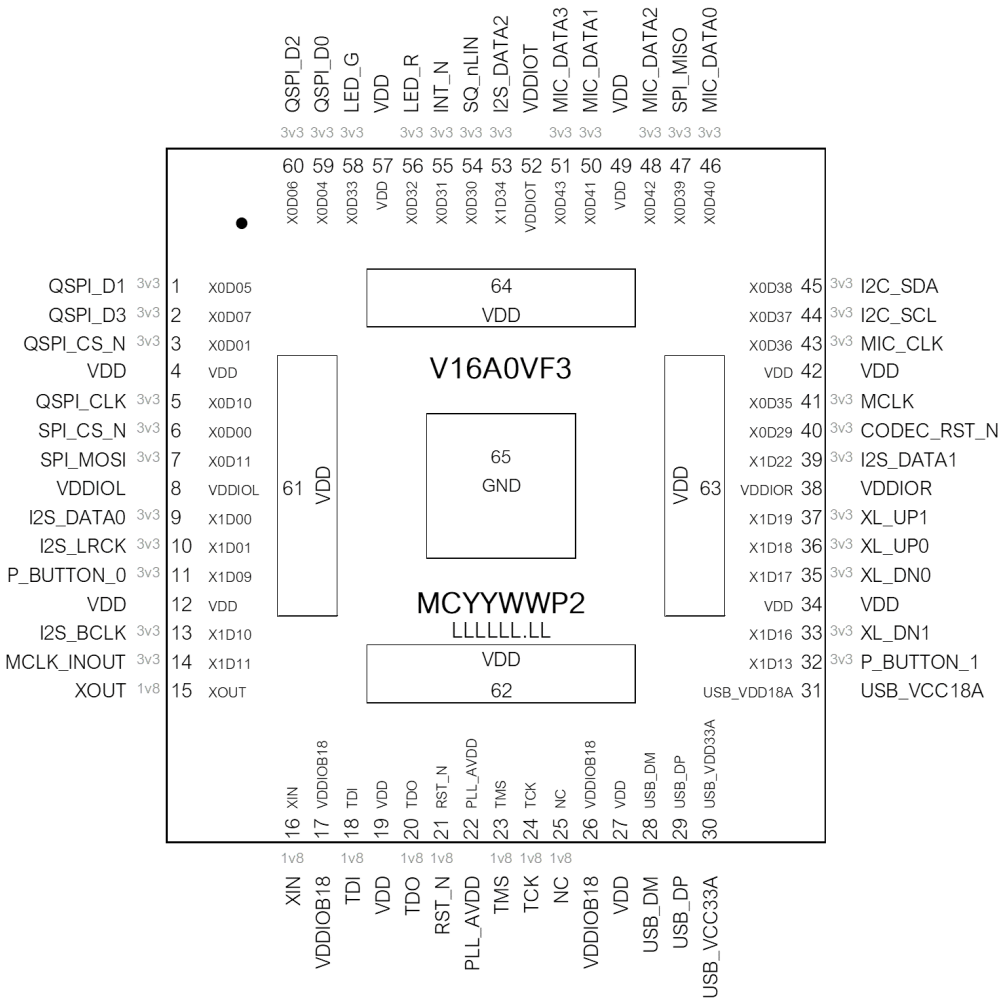
Parameter	Value	Notes
Microphones	4 off PDM	e.g. Infineon IM69D130
Microphone alignment	+/- 2 dB	
Geometry	Linear or Square	
Frequency range	80 Hz to 8 kHz	
Sampling rate	16 kHz	
AEC tail length	192 ms	
AEC reference channels	1 mono	Output to DAC
Double talk detection	Continous	
Reference delay	0 to 500 ms (fixed)	Align microphone & reference signal
Number of beams	3	2 focused + 1 scanning
Beamformer angle	360 degrees	
Noise suppression	up to 25 dB	depending on input SNR
Operating distance	0.3 m to 5 m	
Beamformer update time	16 ms	
Input delay	min 58 ms	Microphone In to I^2S out
Output delay	typ 50 ms	If far end processing on device is implemented
I^2S or USB rate	16 kHz or 48 kHz	Firmware options
I^2S sample bit depth	32 bits	
Input USB sample bit depth	16, 24 or 32 bits	Firmware options
Output USB sample bit depth	16, 24 or 32 bits	Firmware options
Internal PLL range	+/- 1000 ppm	Meets USB Adaptive audio tolerance

Additional information on the operation of the audio pipeline and the control interface can be found in the XVF3800 User Guide.

4 Device Pinout

4.1 Pin Configuration

The pinout of the XVF3800, including all optional interfaces, is shown in the figure below. Some of the pin descriptions indicate how these pins are allocated on the XMOS XK-VOICE-SQ66 development kit (DVK), but they can be re-configured in the firmware for other uses.



VDDIOT, VDDIOL and VDDIOR must be connected a 3V3 supply. VDDIO18 must be connected to a 1V8 supply, and all VDD pins must be connected to a 0V9 supply. All package paddles (pins 61 through 65) must be connected. It is advised to place a via under each paddle to connect it directly to a PCB supply plane.

4.2 Signal Description

The table below lists the functions of all the pins above in the order they appear around the package.

Table 4.1: XVF3800 QF60B Pin Table

Pin#	Pin name	Signal name	Description	Comments	Direction	Power rail
1	X0D05	QSPI_D1	QSPI Data Line 1 and boot selection.	If pin is tied high via a 4.7k ohm resistor on startup, the device will start in SPI slave boot mode. If the pin is left floating or connected to a quad SPI D1 pin on a memory device, the device will start in QSPI master mode and attempt to boot from QSPI flash memory.	I / O	IOL
2	X0D07	QSPI_D3	QSPI Data Line 3		I / O	IOL
3	X0D01	QSPI_CS_N	QSPI Boot Flash - Chip Select	Pull high externally to the device using a 4.7k ohm resistor	O	IOL
5	X0D10	QSPI_CLK	QSPI Clock		O	IOL
6	X0D00	SPI_CS_N	Slave SPI boot / Peripheral SPI Master Chip Select	Pull high externally to the device using a 4.7k ohm resistor	I	IOL
7	X0D11	SPI_MOSI	SPI Master Out Slave In		I	IOL
8	VDDIOL	VDDIOL	I/O Power Supply (3V3)	All VDD pins must be connected	PWR	
9	X1D00	I2S_DATA0	I2S Data	Reference input in INT-Device / Output in USB and INT-Host configs	I / O	IOL
10	X1D01	I2S_LRCK	I2S Left/Right clock	48 kHz or 16 kHz clock derived as I2S_BLCK/64	O (master) / I (slave)	IOL
11	X1D09	P_BUTTON_0	Button input 0	Active low with 10k ohm pullup on XK-VOICE-SQ66	I	IOL
13	X1D10	I2S_BCLK	I2S bit synchronisation clock	Configurable for 16 kHz (1.024 MHz) and 48 kHz (3.072 MHz) sample rates	O (master) / I (slave)	IOL
14	X1D11	MCLK_INOUT	Master audio clock	This pin is an output which provides a copy of the internally generated MCLK and must be connected to Pin 41. Optionally on INT-Device builds with the 'extmclk' binary filename extension, it may be an input pin where the MCLK is externally supplied.	I / O	IOL

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Table 4.1 – continued from previous page

Pin#	Pin name	Signal name	Description	Comments	Direction	Power rail
15	XOUT	XOUT	Crystal oscillator output	Note that this pin should be left floating when using the CMOS clock input	O	IOB
16	XIN	XIN	Crystal oscillator input	Alternatively, this pin can be used as a clock input	I	IOB
17	VDDIOB18	VDDIOB18	I/O Power Supply (1v8)	1V8 supply must be connected	PWR	
18	TDI	TDI	JTAG test data input	This pin has a weak internal pull-up. See note on debug headers.	I	IOB
20	TDO	TDO	JTAG test data output		O	IOB
21	RST_N	RST_N	Device reset	Active low. This pin has a Schmitt trigger input and a weak internal pull up.	I	IOB
22	PLL_AVDD	PLL_AVDD	Analogue power supply for core and application PLL.	Use a filtered version of the core supply as per the XU316-1024-QF60B datasheet	PWR	
23	TMS	TMS	JTAG test mode select	This pin has a weak internal pull-up. See note on debug headers.	I	IOB
24	TCK	TCK	JTAG test clock input	This pin has a Schmitt trigger input and a weak internal pull-down. See note on debug headers.	I	IOB
25	NC	NC	No Connection	Not connected. This pin MUST NOT be connected to any net.	NA	IOB
26	VDDIOB18	VDDIOB18	I/O Power Supply (1v8)	1V8 supply must be connected	PWR	
28	USB_DM	USB_DM	USB D- line	May be left floating if USB is not required	I / O	
29	USB_DP	USB_DP	USB D+ line	May be left floating if USB is not required	I / O	
30	USB_VDD33A	USB_VCC33A	3.3V power for the USB transceiver.	May be left floating if USB is not required	PWR	
31	USB_VDD18A	USB_VCC18A	1.8V power for the USB transceiver.	May be left floating if USB is not required	PWR	
32	X1D13	P_BUTTON_1	Button input 1	Active low with 10k ohm pullup on XK-VOICE-SQ66	I	IOR
33	X1D16	XL_DN1	XLINK	The 2 XL_DNx and 2 XL_UPx signals form a single 2-wire xlink connection for advanced debug only	I	IOR
35	X1D17	XL_DN0	XLINK	Debug port	I	IOR
36	X1D18	XL_UP0	XLINK	Debug port	O	IOR
37	X1D19	XL_UP1	XLINK	Debug port	O	IOR
38	VDDIOR	VDDIOR	I/O Power Supply (3V3)	All VDD pins must be connected	PWR	

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Table 4.1 – continued from previous page

Pin#	Pin name	Signal name	Description	Comments	Direction	Power rail
39	X1D22	I2S_DATA1	I2S Data	Audio data out to host processor in INT-Device config. Reference input in INT-Host config. Optional reference input in UA config.	I / O	IOR
40	X0D29	CODEC_RST_N	GPO for driving reset of conected DAC or digital amplifier		O	IOR
41	X0D35	MCLK	Master audio clock input used for generating PDM MIC clock	Audio clock input to tile 0. Connect to MCLK_INOUT (Pin 14).	I	IOR
43	X0D36	MIC_CLK	Microphone clock output	3.072 MHz output to PDM microphones	O	IOR
44	X0D37	I2C_SCL	I2C serial clock	I2C serial clock line for receiving control command from I2C host or controlling DAC (depending on config)	I / O	IOR
45	X0D38	I2C_SDA	I2C serial data	I2C serial data line for receiving control command from I2C host or controlling DAC (depending on config)	I / O	IOR
46	X0D40	MIC_DATA0	Microphone input 0	Single data rate	I	IOT
47	X0D39	SPI_MISO	SPI Master In Slave Out.	Only used when XVF3800 is a SPI controlled device. Not used by SPI slave boot.	O	IOT
48	X0D42	MIC_DATA2	Microphone input 2	Single data rate	I	IOT
50	X0D41	MIC_DATA1	Microphone input 1	Single data rate	I	IOT
51	X0D43	MIC_DATA3	Microphone input 3	Single data rate	I	IOT
52	VDDIOT	VDDIOT	I/O Power Supply (3V3)	All VDD pins must be connected	PWR	
53	X1D34	I2S_DATA2	I2S Data	Optional third I2S data line for forwarding processed far-end in INT-Device config. Connected to aux input on DAC on XK-VOICE-SQ66 to allow SW configurability. May be used as a GPIO when not assigned to I2S.	O	IOT
54	X0D30	SQ_nLIN	GPO to select topology mode of microphones on XK-VOICE-SQ66		O	IOT
55	X0D31	INT_N	GPO for signalling an interrupt to the host		O	IOT

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Table 4.1 – continued from previous page

Pin#	Pin name	Signal name	Description	Comments	Direction	Power rail
56	X0D32	LED_R	Red element of tri-colour LED on XK-VOICE-SQ66		O	IOT
58	X0D33	LED_G	Green element of tri-colour LED on XK-VOICE-SQ66		O	IOT
59	X0D04	QSPI_D0	QSPI Boot Flash / QSPI Data Line 0		I / O	IOL
60	X0D06	QSPI_D2	QSPI Data Line 2		I / O	IOL
65	GND	GND	Ground	All package paddles must be connected. It is advised to place vias under paddles to connect directly to PCB supply planes.	GND	
61, 62, 63, 64	VDD	VDD	Core power supply (0v9)	All package paddles must be connected. It is advised to place vias under paddles to connect directly to PCB supply planes.	PWR	
4, 12, 19, 27, 34, 42, 49, 57	VDD	VDD	Core power supply (0v9)	All VDD pins must be connected	PWR	

Note:

A. All VDD pins must be connected, excluding the USB_VDD supplies which can be left floating if USB is not required.

B. VDDIOT, VDDIOL and VDDIOR must be connected to a 3V3 supply.

C. VDDIO18 must be connected to a 1V8 supply.

D. All package paddles must be connected. It is advised to place a via under each paddle to connect directly to a PCB supply plane.

E. The function of some pins change depending on the firmware configuration loaded during boot.

5 Device Interfaces

The XVF3800 supports a range of interfaces which allows integration of the device into multiple applications.

5.1 Audio Interfaces

5.1.1 Audio Master Clock (MCLK)

The XVF3800 uses a master audio clock (MCLK) to drive the internal pipeline processing.

The MCLK signal can be derived from one of two sources.

1 - Internal MCLK

The MCLK signal is generated internally in the XVF3800 using a Phase Locked Loop (PLL) that uses the I^2S clock or USB frame clock as the timing reference.

Table 5.1: Signal in internal MCLK mode

Signal	Description	Comment	Pin	I/O
MCLK_INOUT	Master audio clock output	Output - Connect to pin 41	14	O
MCLK	Master audio clock	Connect to pin 14	41	I
I2S_BCLK	I^2S bit synchronisation clock	Configurable for 16 kHz (1.024 MHz) and 48 kHz (3.072 MHz) sample rates	13	I
I2S_LRCK	I^2S Left/Right clock		10	I
USB_DM	USB data	UA configuration only	28	I
USB_DP	USB data	UA configuration only	29	I

Note: This mode is the only clock mode supported in the UA configurations. The audio output stream provides the reference signal for the internal PLL.

2 - External MCLK

The host system can supply a master clock to the XVF3800. This signal must be synchronised to the I^2S clock for correct operation. A 12.288 MHz clock frequency is recommended, but this can be modified in the system firmware if required.

Table 5.2: Signals in external MCLK mode

Signal	Description	Comment	Pin	I/O
MCLK_INOUT	Master audio clock input		14	I
MCLK	Master audio clock	Connected to pin 14	41	I
I2S_BCLK	I^2S bit synchronisation clock	Configurable for 16 kHz (1.024 MHz) and 48 kHz (3.072 MHz) sample rates	13	I
I2S_LRCK	I^2S Left/Right clock		10	I

Note: The XVF3800 requires 32b clocks per sample on the I²S interface.

5.1.2 PDM Microphone Inputs

Four standard PDM MEMS microphones should be connected to the MIC_DATA[0..3] pins. The XVF3800 outputs a clock at 3.072 MHz on the MIC_CLK output, which must be fed directly to all microphones. This clock is derived from the MLCK and must be used to clock the microphone PDM output to avoid undefined artefacts in the processed audio stream.

The XVF3800 voice processor has been tested and characterised with microphones in a linear array placed with a 33 mm separation and a square array with a 66 mm spacing. Other spacings with a maximum spacing of 100 mm are possible, but uncharacterised.

These microphones should be connected to the product enclosure in such a way that the acoustic path to each microphone from outside the product is independent. The XVF3800 algorithms are configured as part of the firmware build configuration.

5.1.3 Audio Interface

The XVF3800 supports a flexible set of audio interface types. The specific interfaces of a device is set by the configuration chosen when the firmware image is built.

In INT-Device configurations the XVF3800 operates as an I²S slave receiving a reference audio signal from the host and returning processed microphone signals to the host. This bidirectional flow of audio samples must be synchronised to a single set of I²S clocks, see the table below:

Table 5.3: I²S signals in INT-Device configurations

Signal	Description	Comment	Pin	I/O
MCLK	Master audio clock		14	I/O
I2S_BCLK	I²S bit synchronisation clock	Configurable for 16 kHz (1.024 MHz) and 48 kHz (3.072 MHz) sample rates	13	I
I2S_LRCK	I²S Left/Right clock	48 kHz or 16 kHz clock derived as I2S_BLCK/64	10	I
I2S_DATA0	I²S Data In	Reference audio data from I²S device	9	I
I2S_DATA1	I²S Data Out	Audio data out to host processor	39	O
I2S_DATA2	I²S Data Out	Audio data out to DAC	53	O

The I²S audio samples are transmitted serially with a delay of one I2S_BCLK cycle between the change of I2S_LRCK phase and the start (MSB) of the audio sample for that channel. This the standard alignment for I²S systems.

In UA configurations the audio signals to and from the host system are carried over a USB connection. The XVF3800 operates in USB Adaptive Mode to synchronise with the host. In this configuration the I²S interface operates in master mode to supply the far end audio signal to the DAC driving the speaker. Optionally, the I²S interface can receive a far end audio signal that has been filtered or processed by the DAC. See the XVF3800 Programming Guide for information about how to configure this optional I²S interface.

Table 5.4: I²S signals in UA configurations

Signal	Description	Comment	Pin	I/O
MCLK	Master audio clock		14	I/O
I2S_BCLK	I²S bit synchronisation clock	Configurable for 16 kHz (1.024 MHz) and 48 kHz (3.072 MHz) sample rates	13	O
I2S_LRCK	I²S Left/Right clock	48 kHz or 16 kHz clock derived as I2S_BLCK/64	10	O
I2S_DATA0	I²S Data Out	Audio data out to DAC	9	O
I2S_DATA1	I²S Data In	Optional reference audio data in	39	I

5.2 Integrated USB Interface

The XVF3800 includes an integrated USB 2.0 PHY supporting Audio Class 2.0 running at High Speed (480 Mbps). This interface is used by the USB host to output a far end signal to a DAC and loudspeaker, to receive processed microphone signals from the XVF3800 audio pipeline and to allow the host to control the operation of the device. In this mode the adaptive USB Audio endpoint is used to generate an MCLK synchronised to the USB host output stream rate. This is provided via the MCLK output on the device. In the case of no output stream being available, the MLCK output is set to a nominal 12.288 MHz.

The table below shows the signals required to implement a USB interface using the XVF3800.

Table 5.5: USB connections

Name	Description	Pin
USB_DP	Connect to USB connector	29
USB_DM	Connect to USB connector	28
USB_VDD18	1.8V supply for USB-PHY - May be left floating if the USB interface is not used	31
USB_VDD33	3.3V supply to the USB-PHY May be left floating if the USB interface is not used	30
USB_VBUS_DET	Note: Self-powered operation is not supported by current device firmware	N/A

5.3 System firmware

5.3.1 QSPI Boot Mode

When QSPI boot mode is enabled (default), the XVF3800 enables six QSPI pins and drives the QSPI clock as a QSPI Master.

For further information about the boot sequence refer to the XU316-1024-QF60B datasheet.

5.3.2 Host boot via SPI

The SPI interface can be utilised by a host controller to download the XVF3800 firmware to boot the device. Details of the SPI boot protocol can be found in the XVF3800 User Guide.

To enable the SPI boot from an external host processor, the QSPI_D1/BOOTSEL should be pulled to VDDIO on power-up. This activates the SPI interface, which operates as a slave to the host processor for the transfer of the boot image, which is clocked in with the least significant bit first in each transferred byte.

This is an alternative to using an attached QSPI flash to automatically transfer boot data on start-up.

The SPI pins are shown in the table below.

Table 5.6: SPI signals

Signal	Description	Comment	Pin	I/O
SPI_CLK	SPI Clock		5	I
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	6	I
SPI_MOSI	SPI Master Out Slave In		7	I
SPI_MISO	SPI Master In Slave Out	May be left floating if not required for control	47	O

5.4 Device Control Interface

The XVF3800 has a control framework that can be used to update device parameters and read data from the audio pipeline and the I/O pins.

Three protocols options are supported - USB, SPI or I^2C. The protocol is set as a compile time option when the firmware image is built. Only one protocol can be active in a specific configuration, but the same control commands are available via all interface types.

Warning: Some commands have no effect on device operation if they are not valid for the configuration in use.

A host control application is provided in the firmware release package that implements the control protocol and provides a user interface for the XVF3800 device.

Note: Only one control protocol, USB, SPI or I^2C can be used in a specific implementation. This choice is set in the firmware and cannot be changed during operation of the device.

5.4.1 USB Control Interface

In the UA configuration of the XVF3800, the control interface is available via the USB Endpoint 0.

5.4.2 I²C Control Interface

The I²C slave interface is used to control and configure the parameters on the XVF3800.

The interface operates with the following specifications:

- 100 kbps SCL clock speed
- Register read/write
- Up to 60 byte I²C read/write

The device I²C address is 0x2C, and the pin connections are shown below.

Table 5.7: I²C slave connections

Signal	Description	Comment	Pin	I/O
I2C_SCL	I²C serial clock line for receiving control command from I²C host		44	I/O
I2C_SDA	I²C serial data line for receiving control command from I²C host		45	I/O

5.4.3 SPI Control Interface

The SPI slave interface can used to control and configure the parameters on the XVF3800.

Note: Only one control protocol, SPI or I²C can be used in a specific implementation. This choice is set in the firmware and cannot be changed while the device is operating.

SPI pin connections appear in Table 5.6. For more information on control and configuration of the XVF3800 please refer to the User Guide.

5.5 General Purpose Input/Output

Two input and five output pins are provided to allow general-purpose I/O (GPIO) such as LEDs and button controls. Input pins can be individually read by the host using the control interface and configured to detect edge events. The output pins can be individually set, and they have configurable Pulse Width Modulated (PWM) brightness control with blinking sequences.

The INT_N pin provides a hardware interrupt to the host system to indicate if a GPI has been triggered. The behaviour of this pin, e.g. which GPI, which edge etc, can be configured via the control interface.

The standard allocation of the GPIO pins in the XK-VOICE-SQ66 development kit is shown in the table below, but these can be adapted in the device firmware for other uses if required for a specific design.

Table 5.8: GPIO pin table

Name	Description	Pin	I/O
P_BUTTON_0	Input for 'Mute' button	11	I
P_BUTTON_1	Input for 'Action' button	32	I
CODEC_RST_N	GPO for driving reset of conected DAC or digital amplifier	40	O
SQ_nLIN	GPO for selecting topology mode of microphones	54	O
INT_N	GPO for signalling an interrupt to the host	55	O
LED_R	Red element of tri-colour LED	56	O
LED_G	Green element of tri-colour LED	57	O

For more information on configuring these inputs and outputs, please refer to the XVF3800 User Guide.

5.6 I²C-to-IO expander

The number of input and output pins can be extended using an I²C-to-IO expander. The IO expander can be attached to the XK-VOICE-SQ66 development kit, and the XVF3800 firmware can be configured to use the additional pins for GPIO over I²C.

6 Device Operation

6.1 Electrical and Thermal Characteristics

For electrical and thermal characteristics, including Absolute Maximum ratings please refer to the XU316-1024-QF60B datasheet.

6.2 Power Supplies

The XVF3800 has the following power supply pins:

Table 6.1: XVF3800 power pins

Name	Description	Pin
VDD	Digital core power supply. 0.9 V (nominal)	4 12 19 27 34 42 49 57 61 62 63 64
V_DDIOL	Digital I/O power supply. 3.3 V (nominal)	8
V_DDIOR	Digital I/O power supply. 3.3 V (nominal)	38
V_DDIOT	Digital I/O power supply. 3.3 V (nominal)	52
VDD_IOB18	Digital I/O power supply. 1.8 V (nominal)	17 26
PLL_AVDD	PLL analogue power. This 0.9 V (nominal) PLL supply should be separated from the other supplies at the same voltage by a low pass filter	22
USB_VDD18	Digital supply to the USB-PHY. 1.8 V (nominal)	31
USB_VDD33	Analogue supply to the USB-PHY. 3.3 V (nominal)	30
VSS	Device Ground	65 (Paddle)

Note: A: All VDD power pins must be connected.

B: USB_VDDxx supplies can be left floating if USB is not used.

See also:

The XU316-1024-QF60B datasheet contains further information on power supplies and power on sequencing.

6.3 Clocks

The XVF3800 device has an on-chip oscillator. To use the oscillator, you need to connect a crystal, two capacitors, and damping and feedback resistors to the device as shown below.

Table 6.2: XVF3800 crystal oscillator

Signal	Description	Comment	Pin	I/O
XIN	Crystal oscillator input		16	I
XOUT	Crystal oscillator output		15	O

Fig. 6.1: Crystal oscillator or clock input configurations

Alternatively, the XVF3800 can be provided with a 24 MHz, 1V8 clock input on the XIN pin. The clock must be running when the chip comes out of reset.

Table 6.3: XVF3800 clock signals

Signal	Description	Comment	Pin	I/O
XIN	Master clock (system)	24 MHz 1V8 clock signal	16	I
XOUT	N/C	Leave floating if clock input on XIN	15	O

See also:

For further information, and details on the calculation of R_f and R_d, please refer to the XU316-1024-QF60B datasheet.

6.4 Reset

The XVF3800 device has an on-chip Power-on-Reset (POR). This keeps the chip in reset whilst the supplies are coming up.

See XU316-1024-QF60B datasheet for further information.

Table 6.4: Reset signal

Signal	Description	Comment	Pin	I/O
RST_N	Device reset	Active low	21	I

6.5 Boot Modes

On start-up and after a reset event, the XVF3800 is booted either using an externally connected QSPI flash memory or by transferring a boot image to the device via SPI from a host processor.

6.5.1 Slave Boot Mode

The boot mode is specified using QSPI_D1/BOOTSEL. If this pin is tied high via a 4.7k ohm resistor on start-up, the XVF3800 will enable SPI slave boot mode and activate the pins shown below.

Table 6.5: SPI slave boot pins

Signal	Description	Comment	Pin	I/O
QSPI_CLK / SPI_CLK	SPI Clock		5	I
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	6	I
SPI_MOSI	SPI Master Out Slave In		7	I
SPI_MISO	SPI Master In Slave Out		47	O

6.5.2 QSPI Master Boot Mode

If the QSPI_D1/BOOTSEL pin is connected to a QSPI_D1 pin on a flash device, the XVF3800 will boot from a local QSPI flash in QSPI master mode. The active pins are shown below.

Table 6.6: QSPI master peripheral interface pins

Name	Description	Pin	I/O
QSPI_CS_N	QSPI Chip Select. This pin should be pulled high externally to the device using a 4.7k ohm resistor	3	I/O
QSPI_D0	QSPI Data Line 0	59	I/O
QSPI_D1 / BOOTSEL	QSPI Data Line 1 and boot selection. To activate QSPI master boot mode connect directly to QSPI Data Line 1 on Quad capable flash device	1	I/O
QSPI_D2	QSPI Data Line 2	60	I/O
QSPI_D3	QSPI Data Line 3	2	I/O
QSPI_CLK / SPI_CLK	QSPI Clock and SPI Clock	5	I/O

A READ command is issued with a 24-bit address 0x000000. The XVF3800 expects each byte to be transferred with the least-significant nibble first. Programmers that write bytes into a QSPI interface using the most significant nibble first may have to reverse the nibbles in each byte of the image stored in the QSPI device. When bulk programming flash devices the Quad Enable bit in the flash setting register should be set.

6.6 QSPI Flash Support

When a flash memory device is used to store the firmware for the XVF3800, the minimum storage space required is 2 Mbytes.

Flash devices with the following specifications are supported by the XVF3800 (e.g. Winbond W25Q16JWSNIM).

Table 6.7: Flash device specification supported by XVF3800

Device characteristic	Description	Value
Page size	Size of flash page in bytes	256
Number of pages	Total number of pages	8192
Address size	Number of bytes used to represent the address	3
Read ID operation code	Operation code to read the device identification (ID) information	0x9F
Read ID dummy bytes	Number of dummy bytes after read command before ID is returned	0
ID size	Size of ID in bytes	3
Sector Erase operation code	Operation code for 4 kB Erase	0x20
Sector information	Arrangement of sectors	Regular (all equally sized - 4 kB)
Write Enable operation code	Operation code for write enable	0x06
Write Disable operation code	Operation code for write disable	0x04
Page Program operation code	Operation code for page program	0x02
Fast Quad Read operation code	Operation code for Fast Quad I/O Read	0xEB
Fast Quad Read Dummy Bytes	Number of dummy bytes after setup of fast quad read that data is returned	1
Read Status Register operation code	Operation code for reading status register	0x05
Write Status Register operation code	Operation code for write to the status register	0x01
Write Status Register Busy Mask	Bit mask for operation in progress (device busy)	0x01

6.7 Device Firmware Upgrade (DFU)

Device Firmware Upgrade (DFU) over USB and I^2C is supported for devices that have QSPI flash connected and loaded with a firmware image.

The DFU over USB supports the standard USB DFU class, and it makes use of publicly available host applications.

The DFU over I^2C makes use of the same procedures and a similar protocol as the USB DFU, but the host application is XMOS proprietary.

If the DFU process fails, the boot process falls back to the factory image allowing the user to re-attempt the upgrade. Images loaded via DFU can also be removed allowing the device to revert to the factory image.

The factory image is loaded only after a reboot of the device, either via the DFU host application or by powering the device off and on.

For further information on the operation of the DFU mechanism refer to the XVF3800 User Guide.

7 Switching Characteristics

For clock, reset and JTAG timing refer to the XU316-1024-QF60B datasheet. XVF3800 specific interface timings are detailed below.

7.1 QSPI Master (External flash for boot image storage)

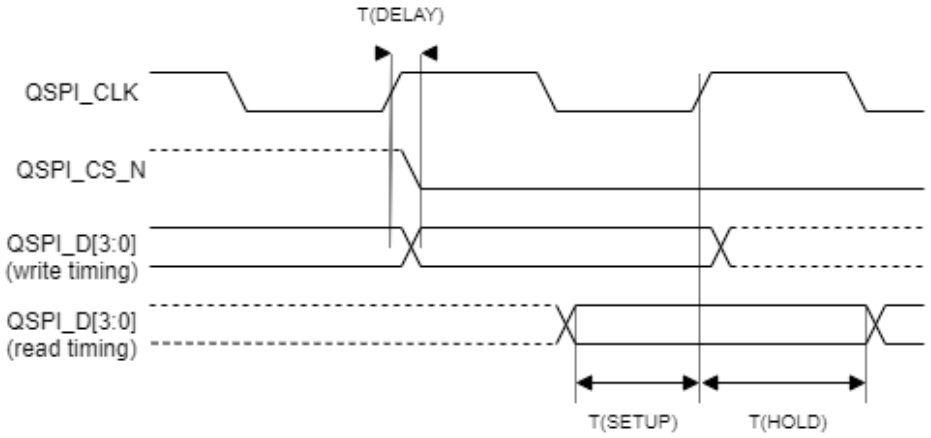

Fig. 7.1: QSPI Timing

Table 7.1: QSPI timing requirements

Parameter	Symbol	Min	Typical	Max	Units
QSPI Clock frequency	f(QSPI_CLK)	-	12.5		MHz
QSPI_CLK to QSPI Data output delay	T(DELAY)	-2.7	-	2.7	ns
QSPI Data input to QSPI_CLK Setup time	T(SETUP)	22	-	-	ns
QSPI Data input to QSPI_CLK hold time	T(HOLD)	-11	-	-	ns

7.2 I²S Slave

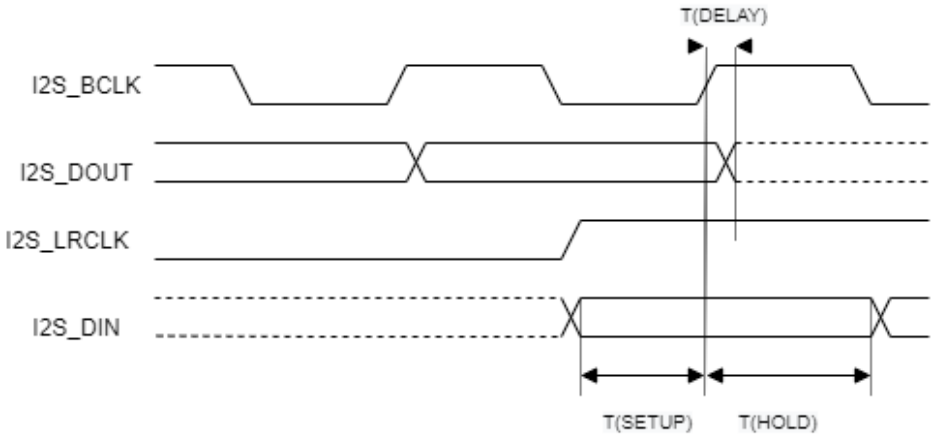

Fig. 7.2: I²S slave timing

Table 7.2: I²S slave timing requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
Master clock input frequency	f(MCLKin)	-	24.576	-	MHz	A
I2S Bit Clock frequency input	f(I2S_BCLK)	-	1.024/3.072		MHz	
I2S Data Input (LRCLK) to I2S_BCLK setup time	T(SETUP)	0	-	-	ns	B
I2S Data Input (LRCLK) to I2S_BCLK hold time	T(HOLD)	6	-	-	ns	B
I2S_BCLK to I2S Data output delay	T(DELAY)	11	-	21.3	ns	

Note:

A: Configurable input multiplier used to generate appropriate audio sample rates (16 kHz / 48 kHz)
B: Dependant on audio sample rate (16 kHz/ 48 kHz)
C: Timing also applies to I²S sample clock (I2S_LRCLK)

7.3 SPI Slave (External processor boot)

Table 7.3: SPI slave timing requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SPI Clock frequency	f(SPI_CLK)	-	12.5	50	MHz	
SPI_CLK to MISO output delay	T(DELAY)	11	-	21.3	ns	
SPI Master Output Slave Input (MOSI) to SPI_CLK Setup time	T(SETUP)	0	-	-	ns	
SPI Master Output Slave Input to (MOSI) SPI_CLK hold time	T(HOLD)	6	-	-	ns	

Note: A: Timing also applies to SPI Chip Select input (SPI_CS_N)

8 Package information

The XVF3800 is supplied in 60 pin QFN package 0.4 mm pitch with additional paddles underneath for VSS and VDD supplies.

8.1 Package Dimensions

The physical dimensions and pin configuration of the XVF3800 device is shown in the figure below:

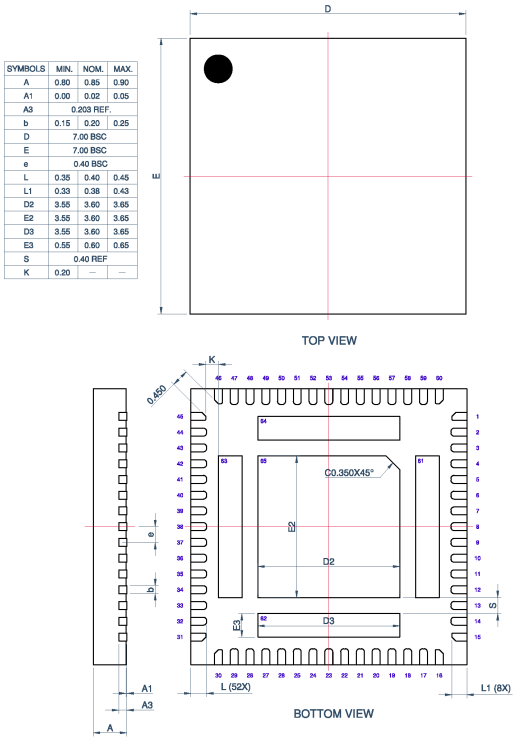

Fig. 8.1: Package Dimensions

8.2 Device Markings

XVF3800 specific device markings are shown below. Only XMOS parts marked with the V16A0VF3 product code are compatible with and licensed to be used with XVF3800 firmware.

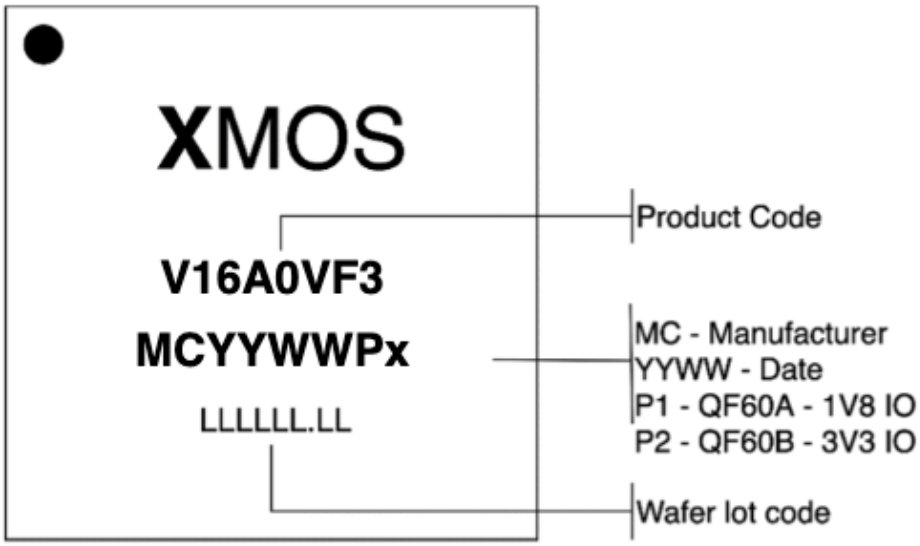

Fig. 8.2: XVF3800 Package Marking

8.3 Moisture Sensitivity Level

The package moisture sensitivity level rating is MSL-3. Devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30 ° C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification for Non-hermetic Solid-State Surface-Mount Devices (J-STD-020 Revision D).

8.4 Hazardous Materials

This product complies with the Reduction of Hazardous Substances (RoHS) directive.

For details refer to https://www.xmos.com/environmental.

8.5 Order Codes

Table 8.1: Ordering codes

Product code	Marking **	Description
XVF3800-QF60B-C	V16A0VF3 MCYYWWP2	Commercial Temp range (0 – 70 ° C) - 3.3V IO

Note: ** MC – Manufacturer, YY – Year code, WW – Week code